
9. FRONT END ELECTRONICS

9.1 INTRODUCTION

9.1.1 Readout electronics overview

Readout of the CMS hadron calorimeters is realized through a chain of system elements beginning with photodetectors coupled to light produced in the calorimeter detection media and ending with memory storage of digitized results in an on-line processor farm. Electronics systems are located in three different areas of the Point 5 experimental complex: (1) the control room at grade level 150 meters above the accelerator tunnels and caverns, (2) the shielded underground service room about 100 meters radially inward from the beam line, and (3) on or adjacent to the detector in the underground cavern centered around the beam line.

Signal processing functions required of the calorimeter readout electronics chain during colliding beam operations can be summarized as follows:

- a) Analog signal conditioning of photodetector responses
- b) Digitization of conditioned analog signals at the beam crossing rate of 40 MHz
- c) Transmission of digitized values from the detector to the adjacent service room at 40 MHz
- d) Linearisation and conversion of front end results into deposited energy values at 40 MHz
- e) Generation and transmission of filter-extracted first level trigger information at 40 MHz
- f) Pipeline storage of linearised energy values during the first level trigger decision interval at 40 MHz
- g) Buffering of linearised time samples at the average first-level trigger accept rate of 100 kHz
- h) Generation of second level trigger information at 100 kHz
- i) Formatting, organizing and transferring of trigger and linearised time sample data to the event builder at 100 kHz

All of the 40 MHz signal processing operations at the very front end of the system are synchronous with accelerator operations and are phase locked to the beam crossings. The higher levels of the readout system operate at an average "interesting event" rate of 100 kHz and are decoupled from the synchronous, pipelined front ends by a set of derandomising buffers.

Other modes of operation of the readout system, e.g. data acquisition for the light flasher calibration system or determination of pedestal values, are far less demanding. The requirements are easily met by a subset of the capabilities needed for data taking.

9.1.2 System configuration

Partitioning of the readout chain is subject to several important global architecture and space constraints, and is impacted strongly by considerations of maintainability. Environmental aspects associated with placing electronics in the collision cavern or inside the detector are discussed in chapter 9 below. In summary, access could be possible to the regions along the side walls of the cavern on a twice a month basis. For the inner part of the detector access could be possible on a yearly basis with difficulty. The CMS first level trigger system cannot be located on the surface because of the time delays introduced; it is located as close to the detector as possible in the adjacent underground service room. Sufficient shielding is planned so that this area can be accessed during accelerator operations. The remainder of the data acquisition and trigger system is located on the surface due to the limited size of the shielded underground service room.

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The configuration selected for readout of the hadron calorimeter has electronics systems located on the detector, along the side walls of the collision cavern, in the underground service room, and on the surface. Analog signal conditioning and digitization electronics are located at the photodetectors attached to the calorimeter elements, trigger and data acquisition electronics are located in the underground service room, and readout control, formatting, and interfaces to higher levels of the system are located on the surface. High speed data links connect the front end digitisers on the detector to the trigger and data acquisition systems in the underground room at the 40 MHz beam crossing rate, and standard communications links bring the digitized data up to the surface at the reduced rate corresponding to first level trigger accepts. Low voltage power supplies and other utilities are located along the side walls of the cavern.

9.1.3 Front end electronics overview

There are a total of 15,096 readout channels in the system; the breakdown by subsystem is given in Table 9. 1 below.

Table 9. 1
Readout Channels

SYSTEM	SECTION	CHANNELS	TOTAL
Forward	Front	1768	
	Main	1768	
	Outer	328	3864
Barrel	Front	2448	
	Main	2448	
	Outer	2160	7056
End Cap	Front	1152	
	Main	2016	
	Outer	1008	4176

The front end electronics system comprises those components located on the detector in close proximity to the calorimeter photodetectors as shown in Fig. 9. 1 and Fig. 9. 2. These components provide the functions of analog signal conditioning, digitization, synchronization/control, and data transmission. A functional block diagram of the system elements for a three-channel subsystem is shown in Fig. 9.3. A later section of this chapter provides details on the individual components. Performance and reliability risks associated with placing the digitiser portion of the readout electronics directly on the calorimeter, where routine service is problematic, have been evaluated and incorporated into the requirements for reliability.

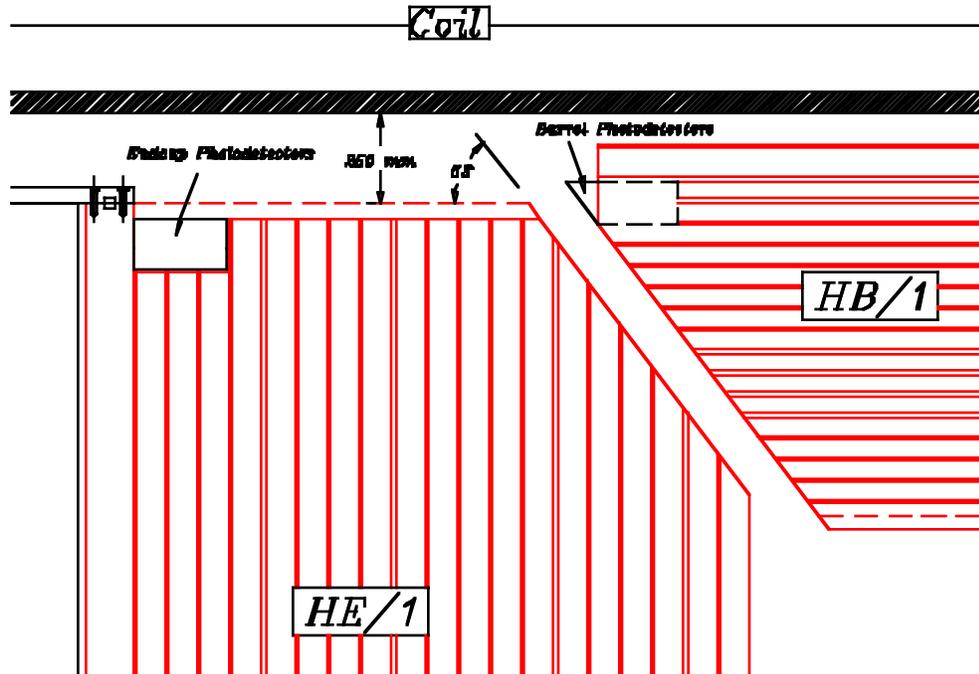


Fig. 9. 1: Barrel and End Cap front end electronics locations

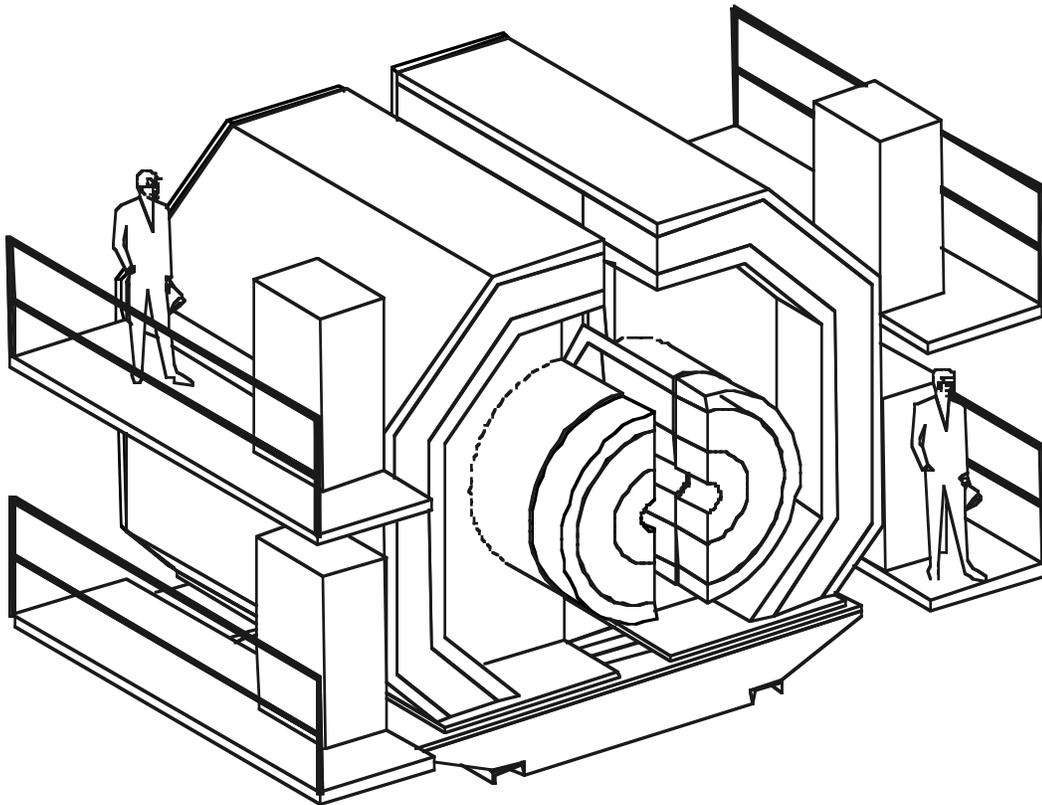


Fig. 9. 2: HF electronics rack locations.

Analog signal conditioning is done using a multi-range current splitter and gated

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integrator, the QIE (Q for charge, I for integrating, and E for range encoding) ASIC. The outputs of this ASIC are 3 bits of range information and an analog level corresponding to the integrated charge on the encoded range. After conversion of the analog level by an ADC, the digitized result is in a eight bit pseudo floating-point format with 3 bits of range (or exponent) and 5 bits of charge (or mantissa). A separate digital ASIC is needed to control and synchronize the QIE channels and to transfer the results over a high speed link to the trigger and data acquisition electronics.

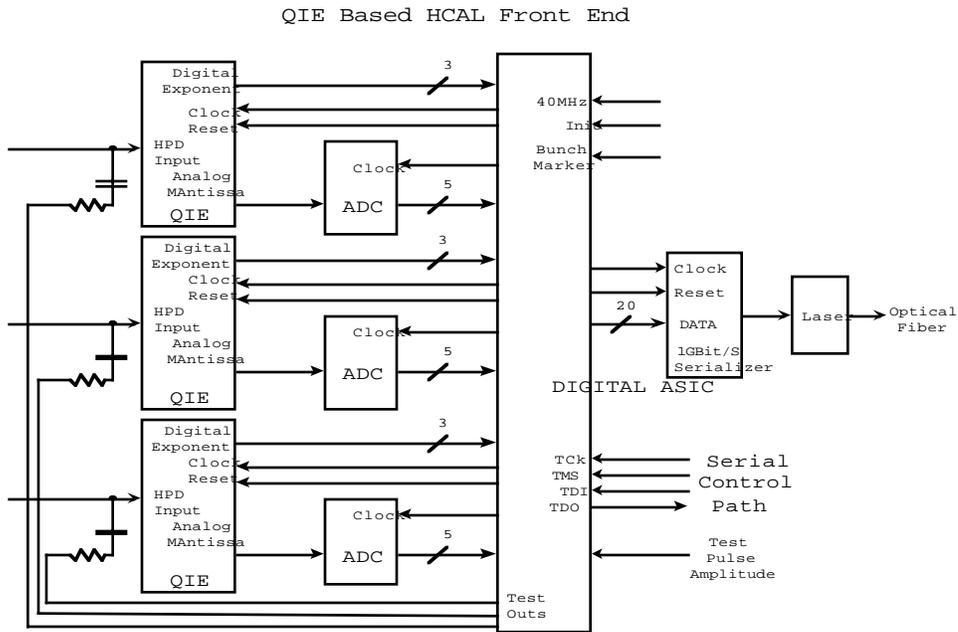


Fig. 9. 3: Front end electronics block diagram.

The front end system operates continuously and synchronously with the accelerator r.f. time structure, 25 ns between beam crossings. Operations are completely controlled by an external clock. A digital value for the energy deposited in every calorimeter channel for each 25 ns interval is transmitted from the front end electronics to the trigger and data acquisition electronics. This 40 MHz clock is provided by a sophisticated distribution and receiver system[1] and includes a synchronization marker which occurs once per orbit of the beam. The marker occurs during the gap in the collider fill reserved for the beam abort function and is used in conjunction with a bunch counter to provide an important check of data validity.

A serial fieldbus, described in chapter 13, is used for communication with and control of the front end systems. Monitor and alarm functions are provided for photodetector high voltages and currents, electronics low voltages and currents, synchronization validity, and temperature values. This fieldbus is also the pathway for exercising test and diagnostic functions, downloading control and parameter data, and selecting operational modes.

Packaging requirements vary according to the location of given calorimeter system. For the inner barrel and end cap systems, custom packaging is needed due to the space constraints as shown in Fig. 9. 1. Small cutouts or pockets are placed into the absorber at the outer radius to accommodate these packages or readout boxes. There is sufficient space for standard crate-based electronics packaging at the forward calorimeter and at the photodetector locations for the

outer barrel and end cap calorimeter compartments.

9.2 REQUIREMENTS

Calorimeter requirements vary over the different regions of phase space in accordance with the physics processes of interest. Missing energy signatures are important for performance requirements in all of the calorimetry, whereas high energy dijet processes mainly challenge the central region calorimeter, and high rate situations are the province of the forward calorimeter. In this chapter, the hadron calorimeter readout requirements are presented in detail over the whole region to define the parameters which set the performance limits. The goal is to define a single set of requirements appropriate to all of the hadron calorimetry and to define a single set of electronics which meets those goals. Considerations driving a single choice involve maintenance and support, stockpiling parts to protect against process obsolescence, economies of scale, and duplication of effort.

9.2.1 Performance

Analog signal conditioning

In the central region, the calorimeter detection elements are scintillators readout with wavelength shifting plastic fibers and the photodetectors are hybrid photodiodes (HPD). The shape of the light pulse produced is an initial step followed by an exponential decay corresponding to the fluorescence characteristics of the combined scintillator-waveshifter system. This time constant, using a single exponential approximation, has been measured to be 11.3 ns. Thus the expectation is that 89.1% of the light signal occurs in the first 25 ns, 9.9% occurs in the next 25 ns interval, and 1.0% occurs in the third 25 ns interval on average. The signal is stretched further when the 5 to 10 ns impulse response of the photodetector and differences in optical path lengths of the elements of a tower are taken into account and convoluted with the light signal; 68% is in the first interval, 29% in the second, and 3% in the third on average. Finally, statistical fluctuations on these average values are significant, especially for the case of low light levels where only tens of photoelectrons are involved.

Since the signals from at least two following beam crossings after the one of interest must be added to obtain the true value, the current produced by the photodetectors must be integrated (and digitized) over each 25 ns interval separately. This is also the case when there is pile up of signals from adjacent crossings as estimating the baseline shift requires charge integral results for several early crossings. Therefore, the central systems require a gated integrator which is reset every crossing, has a precise aperture as close to 25 ns as practical, and suffers negligible charge loss at each 25 ns boundary.

In the forward region, the calorimeter detection elements are quartz fibers directly viewed, and the photodetectors are photomultiplier tubes. The signal produced is due to Cerenkov light from relativistic shower particles, and, as such, is very fast. Test beam results with small, fast phototubes indicate that the entire signal can easily be made to occur in less than 25 ns. Pile up of signals from adjacent crossings thus does not occur, and the pedestal (or baseline depends only on the amount of out-of-time background. Fig. 9. 4 shows a multiple trace oscilloscope picture of calorimeter signals produced by 350 GeV protons.

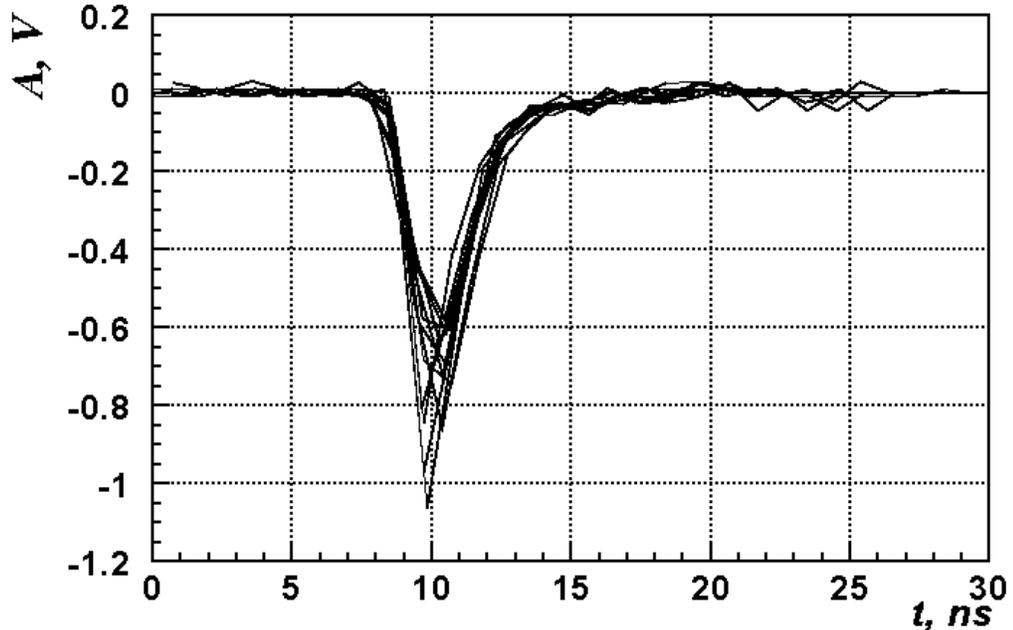


Fig. 9. 4: HF Response to 350 GeV Protons

Given that the signal duration is smaller than the bunch crossing interval, a gated integrator which is reset each crossing is also appropriate for the forward calorimeter. The requirement on aperture precision is modest, 10% is adequate, and the issue of charge loss at the 25 ns boundaries is not relevant to the principal measurement.

Dynamic range

The main compartments of the barrel and endcap calorimeters, HB2 and HE2, are required to respond reliably to minimum ionizing particles in order to contribute to the muon trigger and for off-line identification of muons. This situation determines the details of the low end of the dynamic range and is described below in the chapter on signal to noise considerations. At the high end, studies[2] have shown that the largest energy deposition expected in a central or end cap calorimeter main compartment over 10 years of operation at full luminosity is of order half the beam energy, or 3.5 TeV. Actual jet energies could be higher, but the energy in a jet is spread over several towers spatially and is shared between the electromagnetic and hadronic depth segmentations. In terms of photoelectrons, these requirements correspond to a dynamic range of 1 to 35,000 or 15 bits.

The outer compartments of the central and end cap calorimeters, HOB and HOE, are required to be sensitive to minimum ionizing particles. However, the highest energies seen are significantly lower than those in the main compartments due to the depth at which these layers are located. The physics dynamic range necessary is from minimum ionizing to a rare 1 TeV occurrence. When the photoelectron yield and the low end granularity considerations are taken into account, the requirement is for a 16,000 to 1 dynamic range or 14 bits.

For the forward calorimeter, the single photoelectron signal is extremely important as it corresponds to more than a GeV of energy. Cerenkov light, even when directly viewed, is quite weak in intensity. Test beam studies[3] show that the calibration for the main compartment is approximately 0.4 photoelectrons per GeV. Allowing the upper end to extend

to the full beam energy gives a dynamic range of 1 to 3000 photoelectrons, or slightly less than 12 bits. Providing an extra factor of 4 granularity for single photoelectron performance then gives an overall dynamic range requirement between 13 and 14 bits.

Precision

The precision of measurement requirement, or the granularity of digitization, is set by the energy resolution performance of the calorimeter systems themselves. Resolution is an energy dependent characteristic resulting from statistical fluctuations in shower development and measurement sampling coupled with energy independent effects due to systematic variations in calorimeter response as a function of point of impact or depth of shower initiation. A special case occurs, as noted in the previous chapter on dynamic range, in which the granularity of digitization requirement is determined by a need to measure signal-to-noise values with precision at the low end of the scale.

Energy resolution characteristics of the different calorimeter regions are listed in Table 9. 2 below. A certain functional form is assumed where two terms are folded in quadrature to get the resolution σ :

$$\sigma/E = \frac{a}{\sqrt{E}} \oplus b$$

where, E is the energy in GeV, a is the stochastic term coefficient, and b is the energy independent term to be taken in quadrature with the stochastic value. The values listed are taken from test beam measurements of representative calorimeter structures[3].

Table 9. 2
Energy Resolution Coefficients

Calorimeter	a	b
Central	85%	5%
End Plug	90%	5%
Outer	150%	3%
Forward	200%	3%

The precision of measurement required is therefore an energy-dependent quantity. At very high energies, the resolution limit is about 5% for all calorimeter regions. At very low energies, the requirement for minimum ionizing response or single photoelectron performance also needs a few percent of reading precision. Similarly, for the middle ranges, a few percent of value provides adequate resolution. Precision needed is a parameter that is relative to the size of the signal. Small signals require an appropriately fine precision while for large signals, there is no need for such fine granularity.

Accordingly, the two aspects of precision and range can be separated making the actual requirement one of fixed precision anywhere in the larger dynamic range. The granularity of digitization increases the resolution as the bin size divided by $\sqrt{12}$ must be added in quadrature. For the case of a 10% increase in resolution, from 5% to 5.5%, only 3.5 bits of precision are necessary. At 4 bits precision, the resolution change is 5% to 5.3%, and at five bits the change is only 5% to 5.08%. Thus selection of a 5-bit precision requirement results in negligible

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increase in resolution (performance) from the effect of digitization granularity and provides considerable margin against possible degradation of differential linearity.

The least count requirement is set by the photodetector with lowest gain, the HPD (chapter 8). With gain 2000, one photoelectron becomes 2000 electrons, or 0.32 femtoCoulombs (fC) establishing the minimum granularity.

Noise floor

The signal-to-noise figure of merit is derived from considerations of performance at the low end of the scale. Two different aspects are seen in the calorimeter systems. For the scintillator based devices, the issue is separation of the minimum ionizing particle signal from electronics noise. For the Cerenkov light device, the issue is separation of the single photoelectron response from electronics noise.

The most difficult case for minimum ionizing response occurs in the central region outer detectors where the response is 10 photoelectrons per minimum ionizing particle. High detection efficiency, $> 99\%$, results from achieving a useful threshold at 4 or fewer photoelectrons. A low probability, $< 1\%$, for electronics noise to give a false positive result results from the threshold being 2.33 sigma above the zero photoelectron level. Defining the threshold as 3.5 photoelectrons then sets the noise floor at $3.5/2.33 = 1.5$ photoelectrons. For a photodetector gain of 2000, the noise floor needed is then 3000 electrons rms.

Single photoelectron response is required in the forward detectors. High detection efficiency, $> 99\%$, results from achieving a useful threshold at 2.33 sigma below the mean. For a signal-to-noise ratio in excess of 10:1, this threshold should correspond to 1.5 sigma on the noise. Thus, the single photoelectron response should be $2.33 + 1.5 = 4$ sigma above the zero photoelectron level implying a noise floor of $1/4$ photoelectron. At the maximum photomultiplier gain of 4×10^4 (chapter 8), the noise floor requirement is 10,000 electrons rms. For the expected noise figure of 3000 electrons, the photomultiplier gain could be lowered to 1.2×10^4 .

Cross talk

Cross talk between readout elements can come from several sources; optical cross talk at the photocathode, capacitive cross talk between HPD pixels, and electrical cross talk in the digitisers. Since the signals generated by the coupling mechanisms listed are constant fraction in nature, it is possible to correct the data off-line. Correction is not possible in the trigger systems and a cross talk limit of 2% has been agreed upon. The HPDs have fibreoptic windows which eliminates all optical crosstalk making the cross talk requirement for the readout 2% or less.

Summary

Table 9. 3
Requirements Summary

Parameter	Value
Operation	Gated Integrator
Frequency	40 MHz
Aperture	~25 ns
Aperture Stability	less than 2%
Charge Loss	less than 2%
Range	15+ bits or 35000:1
Precision	5 bits or 0.9% rms
Least Count	2000 electrons or 0.32 fC
Noise Floor	3000 electrons rms
Cross Talk	less than 2%

9.2.2 Calibration*Laser system*

A tree-structure of clear fibers is used to distribute laser light from a central station to each of the photodetectors in the calorimeter system. The principal functions are gain calibration of the readouts and synchronization of the individual channels. Laser light is also sent to a sample of the scintillators to track aging and radiation damage. The frequency with which the laser is pulsed is more than three orders of magnitude lower than the 40 MHz required for beam crossings. No special front end performance requirements are needed over those necessary for event data readout.

LED system

Light emitting diodes are included in each photodetector enclosure for simple viability checking purposes. The frequency of pulsing is arbitrary and could be set high enough to verify the readout capability at the beam crossing rate. The requirements on the front end appear in the area of control functions and are presented in chapter 9 below.

Radioactive source system

A radioactive source traveling in guide tubes can be moved across each of the scintillators in the central calorimeter and is used to establish the calorimeter absolute energy scale. The signal produced in the hybrid photodiode readout is a current of approximately 5 nA. Dark current in the device sets the baseline. Initially this current is in the 3 to 5 nA range, but will increase linearly with radiation exposure to 20 to 30 nA after ten years of operations. The requirement is to measure the source current to 1% of its value on a background that could be as high as 30 nA. The dark current arises from leakage current in the bulk silicon of the diode. It is ohmic in nature (negligible fluctuations) and quite constant in time. In contrast, the signal from the source is quite granular; it is composed of individual photoelectron emissions each

amplified by the HPD gain factor of 2000.

Charge injection

Charge injection directly into the front end of the analog processing ASIC is planned for quality assurance and monitoring purposes. The absolute accuracy of the injection network is not important, but the stability over time is very important. The components involved should be stable at the 2% level for both the ten year planned useful lifetime and the approximately 10^{11} photons and neutrons per square centimeter exposure predicted over that span. Control requirements are discussed in chapter 9 below.

9.2.3 Environment

Magnetic field

All photodetectors and front end electronics are affected by the 40 kG solenoidal magnetic field to some degree. The inner barrel and end cap detectors are immersed in the full field, and are in a region where the field is very uniform. Electronics designs, therefore, cannot use magnetic components such as inductors, relays, fans, power supplies or transformers. In addition, care must be taken to minimize the dipole moment of power leads or to properly brace them against magnetic forces. Testing of electronics prototypes in a 40 kG field is required.

The photodetectors for the outer calorimeter compartments in the central and end cap region are outside of the main detector structure attached to the steel of the return yoke. Fringe fields in this location vary from 500 to 1500 gauss depending on proximity to the service gaps in the return yoke. The field is non-uniform on the scale of meters, but is locally uniform on a scale of centimeters. Unlike the inner detector case, the field strengths are low enough to allow magnetic shielding options to be considered. Magnetic field testing of prototypes is required.

At the location of the forward calorimeter electronics, the fringe field strength is down to a few hundred gauss. Standard crate and power supply systems can be used, although oscilloscopes and other CRT devices will not function there.

Radiation

The radiation environment is most severe in the forward calorimeter system (chapter 5). At the location of the photodetectors, a fully radiation hard chip fabrication process would be required. However, since the electronics is to be located on the outside surface of the shielding encasing the calorimeter, some two meters away from the phototubes, the radiation exposures are expected to be very similar to those predicted for the barrel region electronics. Over a ten year period, the neutron fluences are predicted to be 10^{11} per centimeter squared in both locations. The charged particle dose is negligible by comparison, and the photon fluxes are of the same order of magnitude as the neutrons.

All front end electronics systems are required to withstand this radiation environment and maintain performance levels which meet the specifications in chapter 9 above. Periodic replacements of components over the ten years of operations is not foreseen. Validation of components and/or prototype systems with neutron and photon exposures is required.

Service access and reliability

Forward calorimeter systems are completely separated from the central detector. Access to the electronics mounted on the outer surface of the calorimeter radiation shield is not limited by the CMS detector configuration. The same holds true for HCAL power supply and utility

systems located along the side walls of the cavern and for the barrel and end cap calorimeter components mounted on the outer surface of the magnet return yoke (HOB, HOE). No special provisions are required as service access is straightforward.

The inner barrel and end cap electronics are mounted on the outer radius of the calorimeters inside the superconducting coil. At best, service access could be possible on a yearly basis; a long and difficult disassembly sequence must be executed to gain access to these systems. Even then, repairs are difficult as many layers of cables, cooling pipes, and power leads for the tracking detectors and the electromagnetic calorimeter "trap" the front end electronics boxes and deny straightforward, ready access. These conditions lead to a reliability requirement for the electronics such that single channel failures should be less than 0.1% per year. Also, coupled failure modes which lose an entire box of channels should either be reduced in probability to less than one such failure in the whole system over ten years or be eliminated by engineered mitigations and redundancy.

Cooling

All CMS detector systems in the cavern are required to be cooled; waste heat cannot be dumped into the air. The cooling requirement includes power supplies and power leads as well as the electronics. A large chilled water plant is envisioned. For those cases where it is impractical to remove 100% of the heat generated by water cooling, e.g. a crate of electronics or a power supply, the water system will be operated somewhat below ambient temperature. The subsequent refrigeration of the room air combined with direct heat removal can satisfy the cooling requirement in aggregate.

EMI and EMC

Since the entire electronics plant in the cavern will be operated synchronously at 40 MHz, the potential for EMI problems is great. Second, essentially all of the low voltage power supplies will use switching technologies. And last, ground loops can couple in 50 Hz "hum" and harmonics thereof especially when the loop involves the metal of the detector. Accordingly, the electronics designs shall be compliant with the following guidelines:

- 1) Interconnections of data cables, signal cables or power sources shall not create ground loops,
- 2) AC signal currents, analog or digital, shall not flow through the metal structures of the detector,
- 3) Low voltage power supplies must meet or exceed the European "Electromagnetic Compatibility IEC 1000 - 1-4" specifications for conducted and radiated EMI, plus such additional requirements as developed by the CMS working group on low voltage supplies and grounding,
- 4) The frames (cases) of low voltage power supplies shall be isolated from local detector metal structures with safety grounding provided by the safety conductor of the power cord,
- 5) The techniques used for transmission of digital signals over cables must be approved by the CMS working group on low voltage supplies and grounding,
- 6) Digital circuitry shall be designed in accordance with good engineering practices for control of EMI[4].
- 7) Documentation shall be provided describing the system configuration, interconnects, and grounding.

9.2.4 Control

Event data

During collider operations, the front end electronics runs continuously at 40 MHz under the control of an external clock. Because of differences in time-of-flight, fiber lengths, and photodetector transit times, each channel will require an adjustable phase delay of 64 steps of 0.5 ns size. The fieldbus connection to the Detector Control System will be used for downloading this information to the channels.

Calibration data

Charge injection is foreseen for every channel. The control functions required are:

- 1) Amplitude. The magnitude of the signal should cover the full dynamic range.
- 2) Shape. Two different time structures are needed, a short ~ 10 ns impulse for the forward calorimeter and a longer $RC = 11.3$ ns signal for the barrel and endcap calorimeters.
- 3) Rate. The frequency of charge injection pulses should be selectable from 40 MHz down to 4 kHz.
- 4) Mask. Each channel should have an off/on function
- 5) Phase. The phase for charge injection can be varied using the phase delay control already needed for event data.
- 6) Synchronization. The signal shall be synchronized to the 40 MHz system clock.

Laser light calibrations and scintillator quality monitoring operations will not be synchronized tightly to the 40 MHz system clock due to the jitter in timing of the flashes. Given that beam operations will be off during calibration periods, the transient recorder character of the free running front ends can serve to extract the results. Similarly, the signal produced by the traveling radioactive source is not correlated to the system clock, and higher levels of the readout chain will extract the information from the front end data stream. No special control features are needed.

The LED's used for general viability testing purposes are controlled locally in each readout box. Individual channel controls are not required, except for the phase delay which is already present for event data. Control of the frequency and amplitude of the LED driver are needed.

9.2.5 Error detection and handling

Detection of synchronization slips is needed to guard against misaligned data streams. A 40 MHz counter, reset every beam orbit by the marker pulse, and a comparator should be used for establishing data synchronization validity. Detection of an error results in an appropriate message being sent over the fieldbus to the front end controller in the corresponding trigger and data acquisition crate.

The data links between the front end electronics and the trigger and data acquisition electronics are required to detect and correct loss of synch occurrences. During the interval over which synch is gone, the receiver shall raise an error flag to indicate a bad data condition to the higher levels of the system. The readout pipeline never halts; when corrupted data conditions are detected, the pipeline output is directed to the wastebasket instead of the processor farm.

Sending of test patterns on demand is also a system requirement. The frequency with which this validity check is done has not yet been decided; it will require some operating experience with the links to decide. Possibilities range from once every beam orbit during the

abort gap in the fill to only when needed as a diagnostic tool.

Bit error rates on the links may be such that an unacceptable false first level trigger rate is generated. The solution is to add syndrome bits to each transmission to allow error detection. Such error codes increase the bandwidth requirement for the link and could conceivably increase the bit error frequency. As with test patterns, experience with the links is necessary before the decision can be taken.

9.3 COMPONENTS

9.3.1 Overview

The requirements for the front end electronics detailed in chapter 9 above call for a low noise, high frequency, wide dynamic range digitiser system. In particular, the combination of 3000 electrons rms noise, 0.32 fC least count, 40 MHz clock frequency, and 16 bits dynamic range is unique to the LHC conditions. In the particle physics community, the system which comes closest is the digitiser recently developed for the KTeV experiment at Fermilab[5]. The performance achieved was 15000 electrons rms noise, 8 fC least count, 53 MHz clock frequency, and 16 bits dynamic range. Unlike the LHC case, there were no special requirements on reliability, radiation tolerance, magnetic field immunity, cross talk, and capabilities for DC current measurement.

The front end electronics design is based on an improved version of the analog processing ASIC developed for the KTeV experiment. As shown in Fig. 9. 3, the building blocks are the analog ASIC, a 40 MHz digitiser, a control ASIC and an optical link. Because of the extreme space constraints present in the barrel and end cap regions, a three channel format has been selected as indicated in the figure. Each of the components is described in the following chapters.

Analog processing is done through a multi-range gated integrator. An example of range and resolution performance using a 5 bit ADC and an eight range integrator is shown in Fig. 9. 5. The resolution of the central calorimeter is plotted versus energy along with the contribution from electronic noise at the 1.5 photoelectron level and the contribution from the multi-range front end digitiser system with range parameters as given in Table 9.4.

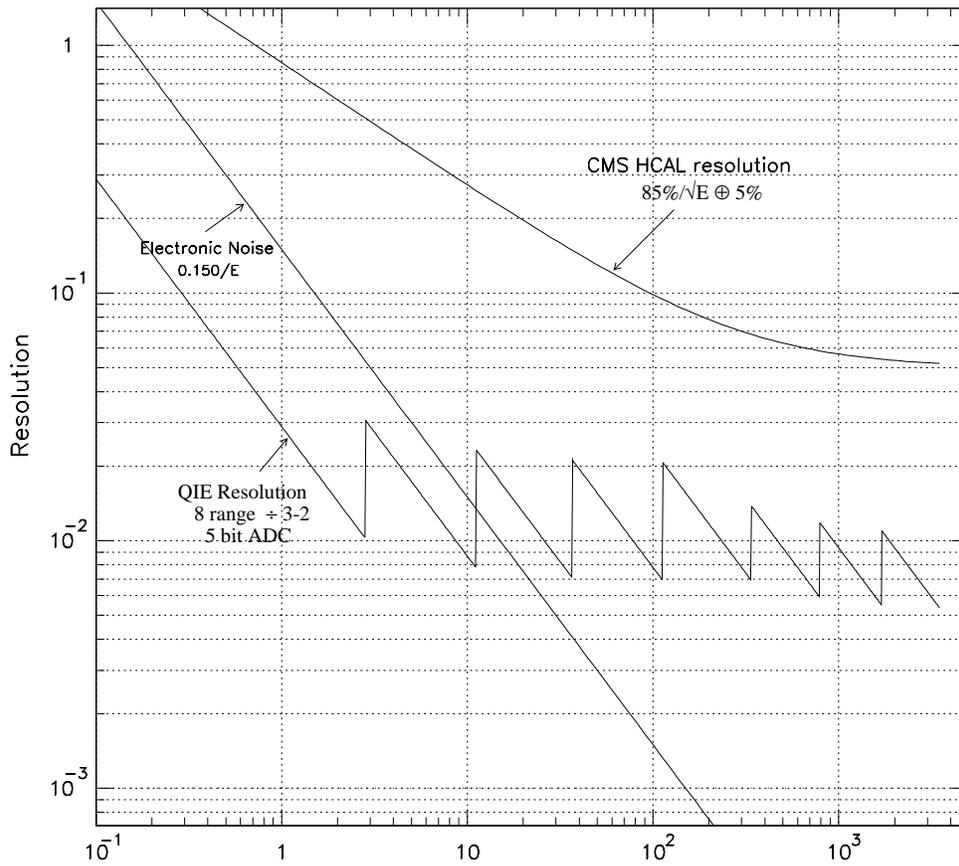


Fig. 9. 5: Resolution performance

Table 9. 4
Range and Resolution Example

Range	Current	Min E GeV	Max E GeV	#Bins	bin size GeV	bin size fC	Resolution Increase
1	I	0	2.8	28	0.1	0.32	1.001
2	I/3	2.8	11.2	28	0.3	0.96	1.002
3	I/9	11.2	36.4	28	0.9	2.88	1.004
4	I/27	36.4	112.0	28	2.7	8.64	1.010
5	I/81	112.0	338.8	28	8.1	25.92	1.024
6	I/162	338.8	792.4	28	16.2	51.84	1.020
7	I/324	792.4	1699.6	28	32.4	103.68	1.020
8	I/648	1699.6	3514.0	28	64.8	207.36	1.020

9.3.2 Analog conditioning ASIC - QIE

Requirements summary

- 40 MHz operation
- 16 bits dynamic range
- 2000 electrons or 0.32 fC least count
- 3000 electrons rms noise
- 5 bits precision
- Systematic errors small enough to measure a few least count source current
- Charge loss at sample boundaries less than 2%
- Cross talk less than 2%

QIE overview and experience

QIE is an acronym for the functions of the ASIC, Q (charge) I (integration) and E (encode). A large dynamic range is accomplished[6] through a multi-range technique. The input current is simultaneously integrated on all ranges, and comparators are used to select the lowest range that is not at full scale. The outputs are a voltage representing the integrated charge plus a three-bit gray code indicating the range. Operations are time multiplexed and pipelined to allow signals to settle and to make the reset interval the same as the integration interval. Latency is 100 ns as the pipeline is four clock cycles deep.

The QIE contains multiple sets of eight capacitors of a uniform value. Attached to this structure is a current splitter. Matched transistors in common base configuration and connected in parallel will share the current driven through them equally. This property is exploited in the QIE design to apportion a fixed fraction of the input current to a given capacitor in the array. Each capacitor receives a fraction of the current of its lower range neighbor. For example, if the splitting was simply by powers of two, the capacitor for range n would receive $1/2^n$ of the input current. Fig. 9.6 shows the pattern of transistors for a single-stage binary-weighted splitter with eight ranges.

Conceptual Drawing of an 8 Range QIE Input Section

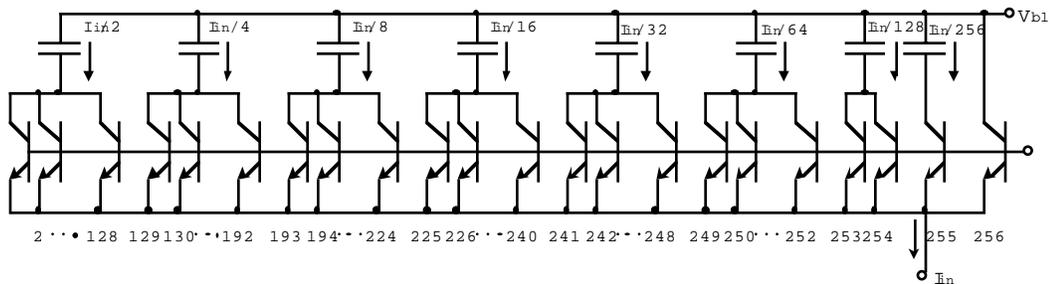


Fig. 9. 6: Input section example for an 8 range QIE.

One set of capacitors integrates the input current for one beam crossing interval; the clock frequency is equal to the beam-beam collision frequency. While one set of capacitors is collecting charge, others are being read out and reset. There are four sets of capacitors. At any given point in time, one set is collecting charge, one is settling, one is being read out, and one is being reset.

A DC bias current is added to the input current. One of the functions of the bias current is to provide a minimum current in the splitter to ensure that the transistors are in a good operating

region. The current is then adjusted so that the analog output on the range of interest matches the input requirements of a single-range ADC. For a given charge deposition over one clock interval, no more than one capacitor in the set will have its voltage within specified limits. The voltage on this capacitor is connected to the analog output of the device and digitized by an external ADC. The priority encoded address of this capacitor make up the exponent bits. The voltage on the capacitor is the mantissa and the address of the capacitor is the exponent.

The QIE is presently in service on the 3100 channel KTeV cesium iodide crystal calorimeter. CsI has an intrinsic energy resolution approaching 0.5%, which requires very high performance electronics to make full use of this capability. The KTeV device has 8 ranges with a factor of two gain change between ranges giving a dynamic range of 16 bits. Fig. 9. 7 shows the results of a laser calibration of a QIE chip carried out at 53 MHz; the scatter in the points is due to photostatistics. There are a number of distortions in the transfer function of this device. The main contributions to the non-uniformity in the overall charge to voltage slope are variations in the size of the capacitors and accuracy of the splitter. Although this is a less than 0.7% effect, KTeV keeps four sets of calibration factors for each QIE, which amounts to 64 constants, four sets of 8 slopes and 8 offsets.

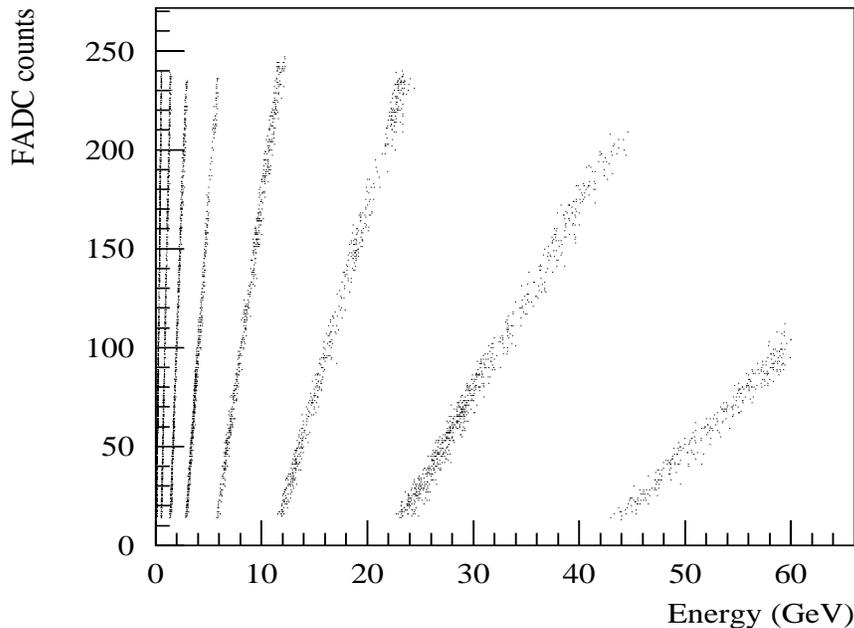


Fig. 9. 7: Laser calibration of a QIE chip.

HCAL design

For HCAL, a modified and improved version of the QIE is planned. The radiation tolerance requirement, the need for extreme reliability, and the operational advantages of a low power design all argue for migrating away from the present 2.0 micron CMOS process. A deep submicron BiCMOS process is under consideration, but the radiation effects are not fully understood at this time. As is the case for all electronics located deep inside the detector, validation of the appropriate level of radiation tolerance is required.

Modifications to the input stage to achieve lower impedance are necessary because of cross talk concerns. The individual anodes in the multi-anode hybrid photodiode detector are

capacitively coupled to their neighbors. A signal on a given element will cause a voltage excursion on the adjacent elements that is determined by the QIE input impedance and the inter-element coupling capacitance. Overall, cross talk to adjacent elements is to be less than 2%.

The noise specification of 3000 electrons rms requires approximately a factor of five improvement in performance. The source capacitance for the CMS HPD and the KTeV photomultiplier tube are roughly the same, $\sim 5\text{pF}$. Thus the improvement must come from circuit design and process technology.

At the time the modified QIE design begins, consideration will be given to bringing the ADC onto the ASIC. The advantages include; lower power as analog drivers and receivers are eliminated, increased reliability from reduced component count, and possibly a lower noise figure. Information will soon be available from a QIE chip designed for the CDF upgrade shower maximum detector which has a 5-bit ADC on board. The noise and frequency specifications are more relaxed than needed for LHC, but the feasibility issues will have been addressed.

Vendor aspects

The practicality of the KTeV QIE is limited by the relatively crude 2 micron CMOS process used for fabrication. The promise of a high performance BiCMOS process for fabrication of the next generation device should simplify using the QIE from a system point of view. KTeV suffered through a series of fabrication quality assurance problems, something that should not occur if a good foundry is used. Nevertheless, KTeV is achieving remarkable performance even with this less than ideal device. They have equivalent dynamic range to that required by CMS HCAL and operate at 53 MHz rather than 40 MHz. Further, system problems have been solved, and 3100 channels is a substantial fraction of the 15000 needed for CMS. The running experience of KTeV brought to light many mundane system issues that are only obvious in hindsight.

As discussed above, the fabrication process selected must maintain performance specifications for an integrated flux of 10^{11} neutrons per square centimeter where the kinetic energies are greater than 100 keV. Also, the photon flux is of the same magnitude and the energies range from 400 keV to 2 GeV.

9.3.3 ADC

Requirements:

The digitiser connected to the QIE analog output must be capable of digitizing the stepped output voltage with full accuracy in one clock cycle. Full span slewing occurs frequently, specifically every time a range boundary is crossed. This puts a premium on the input analog bandwidth of the ADC. It should be greater than 40 MHz in order to accommodate this slewing. If we require that the input section settles to 1/4 of an lsb in one 25 ns clock interval, and further, naively assume a two coincident pole response, that implies about 9 time constants are needed. That is 2.7 ns or about a 60 MHz bandwidth for the components in the analog signal path.

Since the radioactive source calibration current is to be measured by simply reading a large number of samples, it is important that the ADC bin widths remain constant for the duration of the measurement[7]. In any one measurement interval, the signal is small, only 2 or 3 least counts. It is likely that the ADC bin widths around pedestal will have to be mapped

using the laser calibration system to meet the accuracy specifications for the source readout.

Vendor aspects

The critical issues are power consumption and radiation tolerance. There are several commercial ADCs on the market that potentially fulfill the requirements. All candidate devices will have to be carefully evaluated and tested for irradiation effects.

9.3.4 Channel control ASIC

Functionality

Data synchronization

The exponent bits come directly from the QIE, while the mantissa comes from the QIE and goes into the ADC and is then digitized. Exponent and mantissa data appear at different times and need to be re-synchronized before being sent on to the data transmitter.

Clock phasing

The channel control ASIC supplies clock signals to the QIE and ADC. An adjustment is needed for each channel to synchronize operations to the beam generated calorimeter signals. This phase adjustment can remove differences in photodetector transit times, timing differences in the QIEs and ADCs, and differences in light arrival times down the fibers. There is sufficient range to time in all HCAL channels using only these electronics delays.

Initialize

The QIE is a synchronous, pipelined device which contains state machines. After power up, it is necessary to place all the QIEs in a known state with a precision of one 40 MHz clock cycle. The channel control ASIC is required to receive an essentially asynchronous system reset pulse and synchronize this signal to the local clock before sending it on in order to meet the set up and hold times for the reset input of the QIEs.

Data formatting

The QIE + ADC pair produces 3 + 5 or 8 bits of data at the 40 MHz rate. Standard high speed data serialiser chips typically operate on 16 bit data at 66 MHz. This bit rate is a good match to three channels' worth of data. The ASIC can multiplex the incoming 24 bit data into a 16 bit stream at 1.5 times the collision rate or 60 MHz. Should CRC error codes prove necessary, the link frequency can be set to 66 MHz affording enough additional bandwidth to include two syndrome bits. It should only be necessary to protect the exponent bits. Three exponents are nine bits with two bits of error correction. One word at a time, two bits cannot be used to detect more than single bit errors. If the correction algorithm spans five words, that is, ten CRC bits are applied to 45 exponent bits, the majority of 2 bit errors and all 1 bit errors are detected. Error correction should be implemented only if it can be convincingly shown that there is any net improvement in system reliability.

Interface with serial links

The channel control ASIC is the logical place to implement test and control functions by means of a serial link. These functions would include data test patterns, clock trim values, charge injection control, and the control of operating modes. Internal states of the device can be examined as part of a power up diagnostic for example. The widely used CAN standard has been selected for the serial path.

Event synchronization

It is important to identify the crossing from which an event originated. A counter clocked at the crossing rate and reset with the beam turn marker can detect synchronization errors. Subsequently, an error message is sent using the serial link. It is also important to reset, globally, all crossing counters to a known value, and the system must be fast enough to achieve this in one clock cycle on receipt of the bunch marker.

The crossing counter along with a turn counter could be used to specify the time of a test injection pulse. A pair of registers in the ASIC could be loaded with turn and crossing values. If test pulse injection is enabled, then every “n” turns at crossing “m” a test pulse could be issued.

Charge injection and LED trigger

Charge injection and LED test and calibration operations are synchronized to the 40 MHz clock. A DAC and clock counter can provide the signal, and the counter can also serve as a way to turn individual channels on and off.

9.3.5 Data links

Requirements

The CMS trigger system needs information about every crossing. At 40 MHz x 8 bits, 320 Mbit/s per channel is required. This data must be sent 100 meters to the trigger system. An initial comparison of the cost of copper ribbon cable with parallel data transmission at 40 MHz with that of serial optical transmission at 1 Gbit/s shows the ribbon cable to be approximately twice the cost of the serial transmission scheme. It must be noted that data transmission technology is rapidly evolving. Both copper and optical fiber transmission technology are dropping steadily in price while the available bandwidth is increasing. Three channels produce 960 Mbit/s of data which is a good match to present day 1 Gbit/s links. We will carefully watch commercial developments in order to use the trends which develop.

Laser transmitter

There are a number of 1Gbit/s serialiser chips available. It may be for reasons of radiation hardness that GaAs devices are to be preferred. Most of these chips take in a 20 bit word at a 66 MHz rate. The 20 bit word is the result of applying an 8b-10b encoding scheme for 16 bits of data. Clocking the serialiser at 60 MHz or 1.5 times the crossing rate gives the necessary bandwidth to send three eight bit channels on one link. If additional status or error detection bits need to be added to the data stream, it is possible to insert one additional word out of 10 if the link were run at 66 rather than 60 MHz. TEL or GTL I/O levels would be preferable to ECL or PECL levels for reasons of power consumption.

There are a limited number of commercial sources of packaged units which include the laser driver, mounting of the laser and the mechanical housing which enables the coupling of the optical fiber to the face of the laser. For distances of 100 meters, lower cost multi-mode fibers can be used. Their larger diameter also makes the installation into the drivers somewhat easier, although in comparison to copper connections, optical terminations are more difficult. The transmitter is the single most expensive item on the front end boards. If past history is any guide, transmitters will cost substantially less in three or four years' time.

PIN diode receiver

Typically, the firms making the laser module also make the companion fiber optic PIN diode receiver module. Though less costly than the laser, the receiver is still expensive. It too can be expected to come down in price at a rate comparable to the laser modules.

As with the laser and PIN diode modules, most vendors of serialisers make the de-serialisers. It would make sense to use a transmit/receive pair by the same vendor to make sure the serial data stream is compatible.

Link error handling

The 8b-10b encoding scheme which ensures the proper link duty factor also provides some degree of error detection for the integrity of the link. Illegal bit patterns can be detected at the receiver. Commercial modules using this protocol provide a link error output signal which can be used by the data acquisition system to discard events.

9.3.6 Quality control, assurance and monitoring

QA/QC process

The electronics design and development process follows a well known and often used QA/QC process. A complete set of requirements are developed first and then formally approved by technical management. Subsequently a design proposal is developed and reviewed against the specifications. Some R&D is usually part of this step in order to demonstrate feasibility. The design proposal is accompanied by a high level estimate of the cost and schedule impact. Third, a detailed plan of work, a full schedule with appropriate milestones, and a very detailed cost breakdown are prepared. These last items are used to monitor and guide the project to completion and for reporting to oversight groups.

Components

During wafer fabrication of the final designs, there are test structures placed on each wafer for verification that process specifications have been met. It is not clear what sort of tests will be made available to us by the foundry, in light of the small numbers of devices we are having made. Low frequency digital test vectors may be the only tests available. Perhaps more sophisticated tests, including analog voltage profiles will be available because of our participation in CMS.

During the design phase, particularly for the mixed signal devices, several test structures will be needed. The current splitter is an obvious example of something that will need to be characterized. Other structures for tests of radiation hardness will also be needed. Presumably representative structures from many CMS sub-systems can be made on one wafer. This wafer can then be irradiated.

A comprehensive, turnkey test setup was built for KTeV. At least two sets of 3000 QIE chips were run through these testers. Tests were run on the chips before and after their assembly onto a PC card. Analysis of the impact of die yields shows that for yields of less than 98% component level testing is required. The initial yields from Orbit Corp. on the KTeV QIE were of order 70%. It is unlikely any vendor can provide dice with 98% yield.

Commercial components have the advantage of comprehensive testing prior to delivery. Board level testing should be sufficient.

After initial assembly, but before operations with beam begin, the readout system can be monitored and tested in several ways. The most useful are charge injection and the LED's. With charge injection, the full dynamic range can be tested, and the LED's can test viability at the beam crossing rate. Many commercial ADCs have built in test features such as bit pattern generation. This feature is useful for monitoring the data links by running through all possible bit patterns.

9.4 ASSEMBLY AND INSTALLATION

9.4.1 Barrel and endcap readout boxes

Three channel PCBs

The front end digitisers for the HPD signals will be implemented as three channels on a single PCB with 3 QIE chips, 3 FADC chips, digital channel control chip, and an optical link transmitter (Fig. 9.3). Digitized results for the three channels are sent to the trigger and data acquisition system using a serialiser chip and fiber-optic data driver. The 3-channel board must be laid out with no components on the back side and will have to be made as 2 species, a right and a left, as the boards will be laminated to a copper plate which provides a primary cooling path for the electronics. The present estimate for the size of these PCBs is 9 x 9 cm and a nominal FR-4 thickness of 0.157 cm (.062 inches). (FR-4 is used since it is a fire retardant PCB assembly material.) The PCBs will likely be 6 layers with internal power and ground planes for noise reduction. All components on these boards will be surface mounted to facilitate the lamination. It is likely that the boards will be tested for conductivity and then laminated prior to installation of components.

Six-Channel modules

The six-channel modules will be made by laminating a right and left 3-channel PCB to a 0.157 cm (.062 inches). copper sheet which becomes the board support and heat sink. After lamination the assembly will have its connectors for the back plane and other components added. Note: depending on the PCB layout requirements, the lamination may or may not be electrically conductive. It must, however, be thermally conductive. These 6 channel modules are the minimum replaceable unit for on-detector servicing, having a connector to the digital back plane and to the analog input back plane as well as optical data driver connectors on the front of the module.

Backplane interconnections

It seems most likely that there will be 2 separate back planes, (they may be physically the same FR-4 material but will be electrically separated by some amount of space in the layout.) The Digital side of the back plane will provide power distribution, clock distribution, connection to the slow control system, and monitoring services for voltage and temperature. The "analog" back plane will simply provide a connection from the HPDs, which will have short soldered wire leads from their pins to the back plane to the analog inputs to the QIE chips. Communication along the digital back plane is serial data using the "CAN" bus protocol.

Photo detector interconnects

The HPDs have an array of pins on the back which must be connected to the inputs of the QIEs. A socket which matches the pins on the HPD provides a solid ground plane with the appropriate signal return and bypass capacitors. Short twisted pair runs are soldered to

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appropriate points on the analog section of the back plane. This method allows the removal and replacement of an HPD without having to do any unsoldering. The reason for using discreet wires and keeping them short is to minimize the input capacitance to the QIE and to avoid the crosstalk that a ribbon cable might introduce. It is here that we need the full dynamic range, and care must be exercised. After the QIE splitter, noise level constraints are less severe.

External interconnects.

The largest number of external interconnects by far are the fiber-optic data cables, 1 for every 3 channels, which connect the front-ends to the trigger and DAQ system. These connections are made directly to the front of the 6 channel modules using a bayonet style fiber connector. There are also 2 fiber optic cable inputs to the box bringing in the clock and the slow control network. These connect to a special 9x9 cm laminated board structure where the signals are received, processed and distributed on the digital backplane.

Power is brought into the box and onto the back plane using ridged copper bar and threaded stud and nuts with locking washers. These bars must be able to stand the forces experienced due to the magnetic field.

The high voltage for the HPDs is brought onto the HPD socket using a captive bayonet style connector which may be made of molded polycarbonate material and will have mounting screws to prevent accidental disconnection. This connector will also carry the low voltage bias for the HPD.

The last external connection is for the cooling water to the crate. The water lines will be separated from the bundle locally and will be mated to the crate water cooling connectors using a barb and clamp system suitable for use at the flow rates and pressures needed to deliver the 1 liter per minute of cooling water needed to cool the electronics.

Installation.

The readout boxes will be installed on each wedge as the wedge is assembled in Building 168 and will have a full compliment of readout modules installed. This allows for each wedge to be fully tested as a unit prior to installation in the detector. All optical connections from the scintillator tiles are made to the box and each fiber's integrity may be checked using the source system or laser system, thus assuring that all fibers are routed and connected correctly before the wedge is even shipped to the assembly hall.

The mounting of the box and the mounting of the back plane within the box must be of such a design as to withstand the forces due to the magnetic field. Once the wedge is installed in the detector, the real power cables must be installed and appropriately anchored to the wedge. Water lines will then be connected and the final assembly fully tested prior to being sealed up in the detector.

Quality control, assurance and monitoring.

In general, all assemblies will be specified to the vendor to meet the requirements of the final design. PCB manufacturers must meet minimum de-lamination force testing and all PCBs will be "bed-of-nails" tested to assure correct conductivity prior to being accepted. Commercial electronic components will be required to pass needed minimums for voltage tolerance and for radiation tolerance. Sample parts from vendors must be radiation hardness tested before being selected for final assembly.

Custom integrated circuits

It is expected that the full custom chips which will be designed for this application will have a multilevel evaluation process. The first part of this will be to qualify the foundry which will be making the parts for radiation hardness and for process stability. The vendor which will be packaging the parts must also be qualified, although this is somewhat less critical as the choice of packaging vendor may be changed easily, where as the choice of ASIC foundry is much more difficult to change.

The next level of assurance will be to have a series of prototype parts made and tested in parallel with a design review using impartial but interested engineers to make sure that no design flaw is missed. Prototype parts will also be subjected to stresses of radiation and thermal cycling to assure that the part can stand the stresses placed upon them in normal and extreme operating conditions. Note that the cooling system as designed will operate at a temperature slightly below ambient which will keep the parts quite cool and add reliability. Of course, there will be test structures present on each wafer of chips produced; these will be used to monitor the process and quality at the foundry.

Chip testing

Once production parts begin arriving, we will be using the ASIC/Board test system developed at Fermilab to do production testing of the chips. All chips will be tested at speed and will be required to pass stringent cuts on the performance of the part as well as the total current draw. Once parts have passed the chip testing stage, they are shipped to qualified assembly houses which mount the parts to the PCB modules and ship these back for testing. (Note: the vendor MUST adhere to correct ESD protection procedures, as failure to do so may damage or weaken parts which will then fail prematurely.) It is expected that the time to test each chip will be about 20 sec., this includes installing the chip in the test fixture and removal and sorting of good and bad chips.

Board testing

The 6 channel modules will also be tested using the ASIC/Board test system and will again be tested at speed. Also in this test, the cross talk between channels is measured and each channel is required to pass the same performance test as the chips passed. The current drawn by the board will be measured and boards which do not pass the test will be returned for re-work/repair.

It is expected that the time to test each board will be about 2 minutes. This is in part due to the optical connections which must be made by hand to allow for the full testing of the board. The test fixture will have a pseudo-back plane which the board will be installed in during testing.

It is further expected that some number of boards will be subjected to thermal cycling and extended running to elicit expected infant mortality and longevity numbers. It is also likely that all boards will be installed into a burn-in fixture and will be run for several weeks and then be re-tested, again to catch infant mortality of components.

System testing

Since the only active components which are part of the readout box are the HPDs and since they will be tested separately, it is assumed that testing will be done on the wedge as it is assembled. Any additional testing would be redundant and would not add to the reliability of

the system.

9.4.2 Forward readout electronics

VME readout crates

The digitisers for the PMT signals will be implemented on 32-channel boards, 9Ux400mm Eurocard format, with VMEbus signals on the P1 connector (referred to as “VME modules” for simplicity). Each module will consist of a PCB of conventional design, fabricated of 0.157 cm (.062 inches) thick FR-4 material, with SMT components on both sides. It is likely that groups of 3 digitiser channels will be assembled on a small “daughtercard” for ease of assembly and testing, and that 10 daughtercards will mount on a VME module. All components except connectors will be surface-mounted. Front panel hardware and board stiffeners will be Eurocard standard.

Assembly will be performed by an outside vendor, using conventional pick-and place component installation and infra-red reflow soldering. Mechanical components will also be installed by the vendor.

A 9U crate of standard size will house up to 16 VME modules. A standard VME-16 P1 backplane will be installed, along with a power distribution backplane and coaxial ribbon connectors for PMT input signals. An existing standard such as the CERN V430 specification will be chosen for power distribution. The crate will be custom-manufactured to our specifications by an outside vendor.

PMT bases and interconnects

The PMTs are housed in individual shielded enclosures, with a simple PCB soldered to each. The PCB contains the voltage-multiplier portion of a Cockcroft-Walton generator as described in chapter 8. Each PMT base has two connectors, a coaxial signal output connector, and a multi-pin control connector for the high-voltage generator. The high voltage is generated inside the PMT base, so the interconnections themselves are low voltage.

The PCBs for the PMT bases will be assembled and conformably coated by an outside vendor using standard techniques. Final assembly of the PCB to the PMT and installation in the base enclosure will be performed in-house at a collaborating institution’s shop.

Interconnection cables will be manufactured by an outside vendor to CMS specifications, and tested in-house.

External interconnects

This chapter refers to all off-detector connections which leave the HF platform. The majority by number are the fiber-optic data cables. Each 32-channel module has 11 data cables, which are identical in function to those used in HB and HE.

The 220 VAC power is supplied to each rack in a conventional manner. Low voltage is generated in each crate using a conventional power supply. Cooling water is also supplied to each rack. Two fiber-optic connections are required for each rack for the clock (TTC system) and detector control.

Installation

The PMTs with bases will be installed while the detector final assembly is done in the experimental hall. Electronics racks containing VME readout and high voltage control crates

will be installed on the exterior of the detector. Cables will then be run from the PMTs to the racks.

Quality control, assurance and monitoring

In general, the same procedures will be followed as for the remainder of HCAL. The custom ICs will be processed as described there. The VME modules will be tested in a dedicated test station in-house after assembly. Each VME crate will be similarly tested in-house.

9.5 EXPECTED PERFORMANCE

9.5.1 Event data

The front end electronics system is based on a multi-ranging integrator and encoder called the QIE. The system is fully pipelined producing digitized values synchronously with the beam crossings after a latency of 100 ns corresponding to the pipeline length of 4 clock cycles. It is designed to meet the requirements described in detail in chapter 9. Based on the successful experience of the Fermilab KTeV experiment which uses a QIE and a very similar front-end electronics design, the HCAL system is expected meet all of the goals.

The most demanding requirement is the noise floor, $1/2$ of a fC or 3000 electrons rms is the requirement, resulting from the low gain figure of 2000 for the HPD. There are three environmental factors which lend credibility to achieving a 3000 electron noise floor system; (1) the HPDs and the readouts are in fully enclosed copper boxes, (2) the connections to the HPDs are only a few cm long and the bypass network for the silicon diode pixels has a good ground plane, and (3) the only external copper connections to a box are the high voltage and low voltage power leads which are configured with a single point ground at the box.

9.5.2 Calibration data

Light flasher operations, whether from the laser system or the LED system, only occur when beam is off. Thus, there is no baseline shift or pileup correction to be made. Also there is no requirement that the flasher be synchronized to the clock as the front ends function as digital wave form recorders. The higher levels of the trigger and data acquisition system are fully capable of extracting flasher responses. However, it is convenient to synchronize the flashers to the clock to set repetition rates by counting and simplify generation of trigger accepts at the proper time. Synchronization also makes programming of the higher system levels that much easier.

Charge injection calibrations are fully synchronized to the clock in each individual channel control ASIC. As such, operations are identical to those for event data except that the trigger accepts are synchronous.

The requirement to measure the current produced by a radioactive source illuminating the scintillators is challenging. The induced current is about 5 nA after amplification by the HPD. There is a DC leakage current in the silicon diode pixel which starts out also at about 5 nA but increases linearly with radiation exposure and is predicted to be 20 to 30 nA after 10 years of operations. This silicon leakage current is ohmic in character so that the fluctuations are negligible.

Due to the noise floor requirement, adding switches at the very front end to allow for a separate DC current transducer readout path is essentially ruled out. A second negative is the

added system complexity and cost and reduced reliability introduced. The choice is to operate the system in its normal mode at its normal clock speed and measure the small source current through extreme over-sampling[7]. By using the noise in the system and the photoelectron fluctuations of the current to “dither” the signal, it is possible to measure the current to a few tenths of a percent of a least count by averaging over a large number of readings.

Five nA corresponds to an average of 0.4 photoelectrons per measurement. This value also corresponds to 0.4 of the least count as the system granularity on the most sensitive range is one photoelectron per ADC bin. The Poisson probabilities for the number of photoelectrons per measurement are: $P(0) = 67.0\%$, $P(1) = 26.8\%$, $P(2) = 5.4\%$, $P(3) = 0.7\%$, and $P(4) = 0.07\%$. Chapter 11 describes the control functions and configuration of the higher levels of the readout system needed to accumulate and average the readings. The pulse-height spectrum built up by a large number of measurements will be the 0.4 photoelectron Poisson distribution convoluted with a gaussian noise distribution which has a sigma of 1.5 least counts (3000 electrons). The calibration value extracted by fitting the spectrum is the average number of photoelectrons per measurement interval.

9.6 SERVICES AND UTILITIES

9.6.1 Cables, wires and connectors

Barrel and end cap

Front end electronics for the barrel and end cap are contained in readout boxes attached to the detector. There are 120 boxes distributed as shown in Table 9. 5.

Table 9. 5
Number of Readout Boxes

System	No. of Boxes
Inner Barrel	36
Outer Barrel	60
End Cap	24

Each box has power cables, cooling water hoses, 50 data fibers (to be determined), a fieldbus duplex fiber cable, a TTC fiber cable, and a twelve pair high voltage cable.

The power and cooling services are described in chapter 12. Selection of the data fiber interconnects will be done following CMS-wide discussions of commonality between different detector systems. The fieldbus interconnect is a commercial Arcnet hardware, and the TTC link follows the recommendation of the RD-12 group. The high voltage cable has silicon rubber insulation for the pairs, a nonscintered PTFE tape 50% lap, a tinned copper spiral shield, and a halogen-free thermoplastic elastomer jacket.

Connectors for the power leads are bolted copper flags with Belleville tensioning washers. Connectors for the data fibers are to be determined. The Arcnet and TTC links have off-the-shelf connectors which are predetermined by the TX/RX hardware. High voltage cables will use custom multi-pin molded connectors as commercial catalog products are limited to 14 kV. Deep wiping contacts similar to those of "banana jacks" are planned.

Forward

Front end electronics for the forward calorimeters reside in VME crates in relay racks attached to the calorimeter outer shield. Coaxial cables bring the phototube signals out from the interior of the detector through penetrations in the shielding. The high voltage cables (also routed through these passages) are multi-conductor with an overall shield made of the same materials as those for the barrel and end cap systems. Ethernet and TTC services use optical interconnects and commercial technology. Selection of the data fiber interconnects will be done following CMS-wide discussions of commonality between different detector systems. Table 9.6 below gives the count and routing for the interconnects.

Table 9. 6
Cables Required for HF

Count	Function	From	To	Length	Type
3900	PMT HV	HV PS	PMT Box	2m	custom multi-conductor
3900	PMT Signal	PMT Box	FE Card	2m	coax
1300	Digitized Data	FE Card (Rack)	Service Room	100m	optical fiber
16	DCS	Service Room	Crate	150m	optical fiber
16	TTC	Service Room	Crate	150m	optical fiber

9.6.2 Cooling*Barrel and end cap*

Cooling water for the readout boxes is brought in via hoses described in chapter 12. A water temperature rise of about 4 °C is expected for the 210 watt heat load with a flow of one liter per minute. If the supply temperature is set 4 or 5°C below ambient temperature, the system provides some degree of refrigeration to the cavern environment.

Forward

The crates for the forward calorimeter front end electronics are located in relay racks. Standard CMS infrastructure cooling is planned with air-water heat exchangers and forced air circulation. The electronics dissipates 1.1 W per channel. For 500 channels in one 9U VME crate, this is 550 W. An additional 250 mW per channel is needed for the high voltage supplies giving another 125 W for a total of about 800 W when control and processor cards are included. A flow of about 6 liters/min. would give a temperature rise of 5 °C. For the full system then, a flow of 50 liters/min. is required. Because heat is not removed effectively in rack based crate and power supply systems (getting 60 to 70 % into the water is doing well), the entire system will be operated below ambient to provide extra refrigeration to compensate.

9.7 ACCESS, MAINTENANCE AND OPERATIONS**9.7.1 Inner barrel and end cap electronics**

The inner barrel and end cap electronics along with the photodetectors are located in

9. FRONT END ELECTRONICS

water-cooled readout boxes mounted on the outer surface of the calorimeter structures. These locations are inside of the cryostat for the solenoidal coil as shown earlier in Fig. 9. 1. Access is not possible without a long and difficult disassembly of the detector involving the forward calorimeter, the end cap muon detector and return yoke, and the end cap calorimeter. At best, service access could be possible on a yearly basis. Stringent reliability requirements derive from the lack of repair access. Failures at the single channel level must be less than 0.1% of the channels per year, no more than 7 of the 7500 trapped channels. At the system integration level, the relevant time interval is the ten year operating period foreseen. Loss of an entire readout box of 128 channels should occur no more than once in the ten year period.

Repairs and maintenance operations, even after the detector has been opened up, are very difficult as many layers of cables, cooling pipes, and heavy power leads prevent straightforward, ready access to the boxes. Additional time will be needed to disassemble whatever portion of these services are blocking access to that area of the box where the repair is to be done. Simple service activities, changing an electronics card or repairing a high voltage problem could take months to execute. Accordingly, the design of the readout boxes is such that no maintenance is required. All parameter adjustments are made using a fieldbus connection, there are no hand-settable adjustments. The power supplies are in accessible locations in the cavern and the service room. There are no moving parts to wear out. All interconnections are threaded or locking, and the power connections use Belleville tensioning washers to eliminate any need for periodic retightening.

9.7.2 Outer barrel and end cap electronics

The outer barrel and end cap electronics along with the photodetectors are located in water-cooled readout boxes mounted on the outer surfaces of the return yoke. These locations are directly accessible during any routine access into the cavern. There is no issue of residual radioactivity at those locations, but the magnetic field strengths expected, 500 to 1500 gauss, would call for proper procedures, training, and equipment should a service access be made with the solenoid energized.

Having relatively unimpeded access to the equipment makes these electronics systems readily serviceable. However, there are many advantages to using identical readout electronics systems to those designed for the inner detectors. Thus, the outer calorimeter electronics system, like the inner one, would have no maintenance requirements. The reliability goals of the inner system are such that repair accesses should be minimal, once per year or less.

9.7.3 Forward electronics

Electronics for the forward calorimeter are mounted in conventional racks and crates on the detector support platform on the outer surface of the HF shielding. High voltage and signal cables penetrate through the shielding to minimize cable lengths. Fig. 9.3 shows the approximate rack locations. When the detector is in the garage position, the racks are easily accessible for any required maintenance or repair operations. Access is somewhat more difficult in the cavern as the calorimeter is some 8 meters above the floor level centered on the beam line. Specific personnel access techniques, stairs, catwalks, and lifting devices, have not been designed at this time, but are straightforward applications of well-known hardware. The magnetic field strengths expected, a few hundred gauss, would call for proper procedures, training, and equipment should a service access be made with the solenoid energized.

The residual radioactivity activity levels discussed in chapter 5 refer to the end of a ten

year operating period. During commissioning and the early years of accelerator operation, activation will not be a problem and no restrictions on access to the electronics are expected. As the system grows more and more activated, there could be need for placing time limits on access or for temporary local shielding during maintenance operations. Therefore, the forward calorimeter front end electronics system should feature good remote diagnostics to pinpoint problems and allow for simple replacement as the preferred method of repair.

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