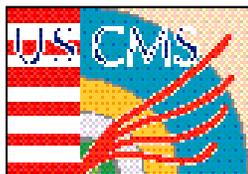


Status of the Endcap Muon Trigger Project

Jay Hauser, *UCLA*

**DOE/NSF Review
August, 1999**



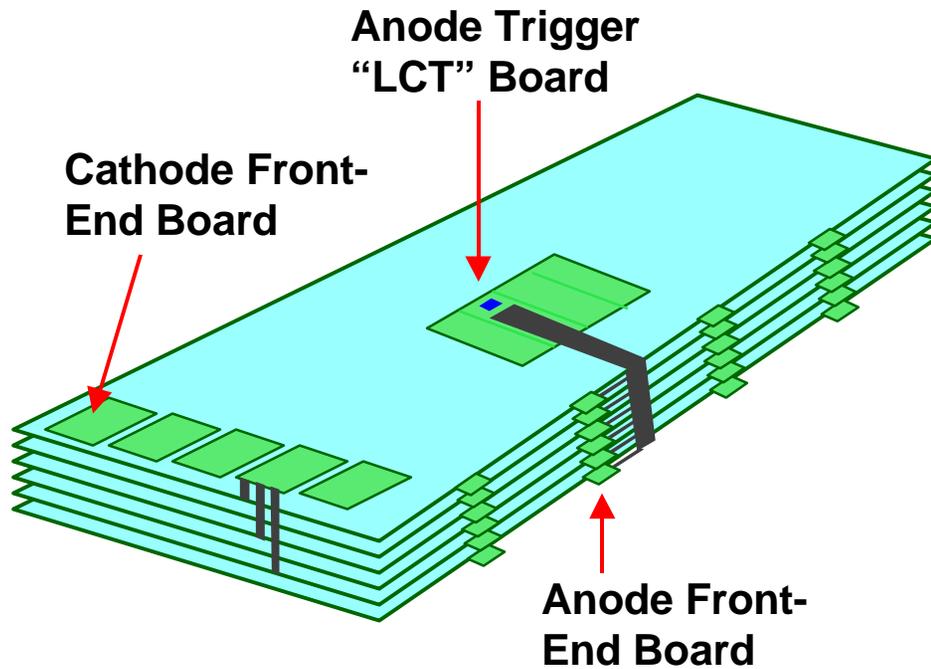
Background Information

- There have been 2 major prototype cycles since the first DOE/NSF review in 6/97 (none previously)
- Performance prototypes:
 - ✓ All on-chamber trigger elements
 - ✓ Tested at CERN in summer 1998
 - ✓ The trigger design criteria were met or exceeded
- Engineering prototypes:
 - ✓ Boards built, to be tested at CERN Aug.-Sept. 1999
 - ✓ Full trigger and DAQ interfaces
 - ✓ Increased density
 - ✓ Lower power
- Design change:
 - Trigger circuitry does not fit on front-end cards
 - Move the electronics to crates on iron periphery

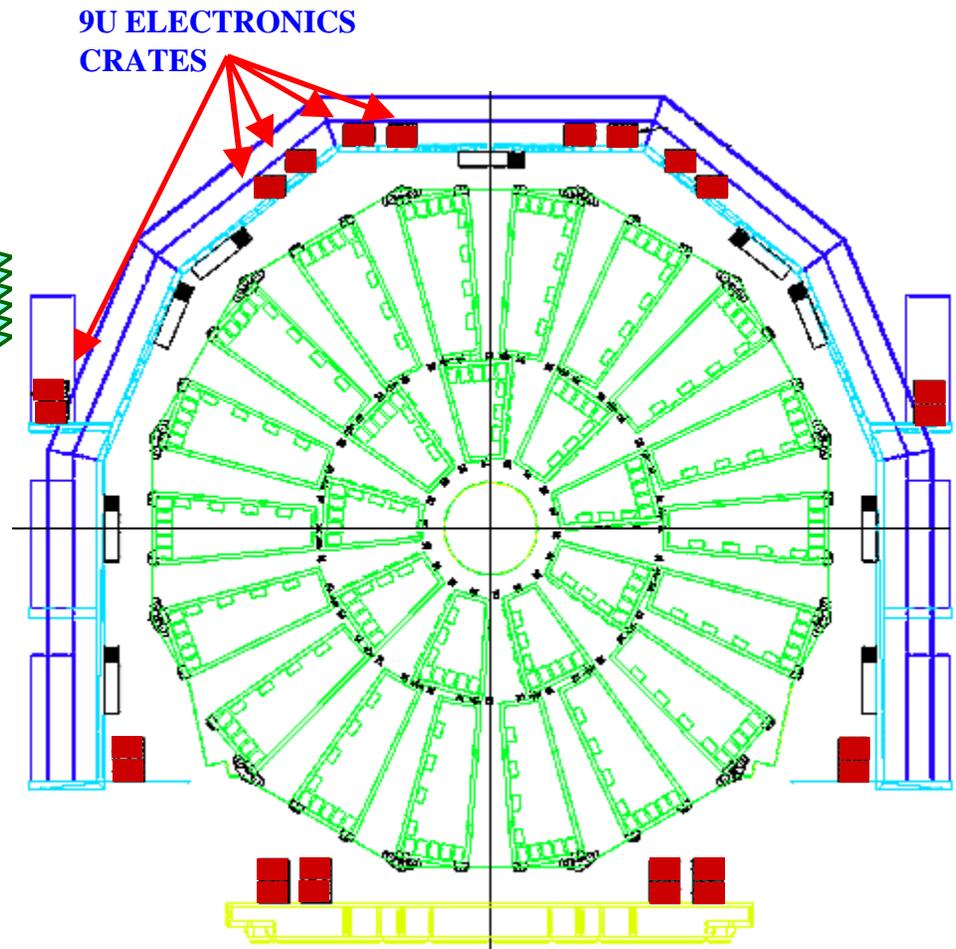


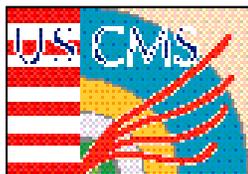
Physical Layout of CSC Trigger Electronics

Single (Large) Chamber



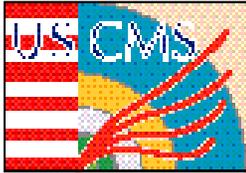
Peripheral Crates





Background Information

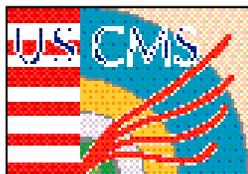
- **Reasons for crates around iron disk periphery:**
 - Lack of on-chamber space (esp. ME1/1, ME1/2, and ME1/3)
 - Power and cooling
 - Access for maintenance and DAQ etc. connection
 - Timescale for installation
- **The proposal to move electronics to these crates was presented to the Feb. 1999 Project review**
 - Close-out report “This change adds significant flexibility, improves accessibility, and saves space in critical areas. Some additional costs will likely be incurred and are being evaluated”.
- **The implications of this design change are becoming well understood:**
 - A straight-forward analysis gave a total cost increase of \$3.5M
 - Cost optimization has reduced this to an increase of \$1.71M
 - The largest single increase (\$0.94M) is for “LCT” circuitry



Summer 1998 Beam Tests

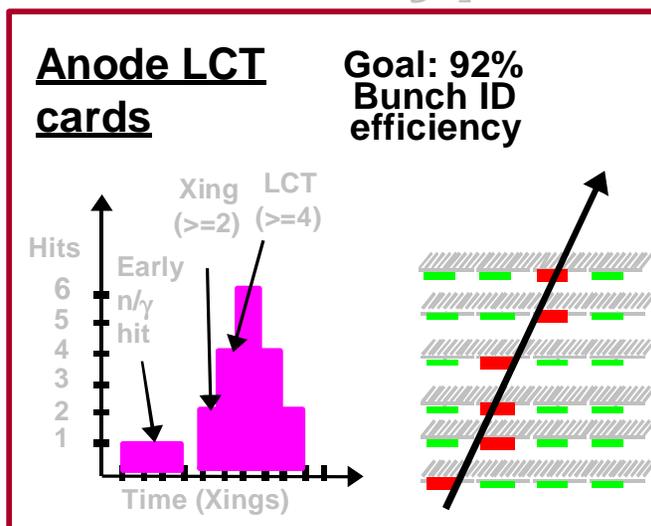


Full Scale 1:1 Large Chamber - ME2/2 or ME3/2

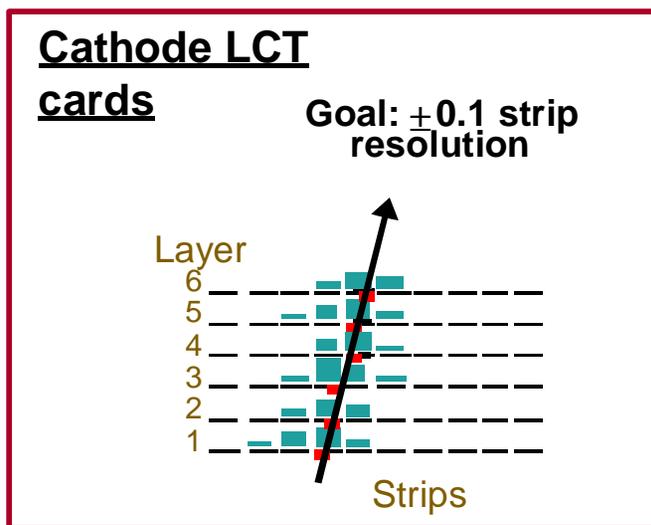


Focus for Muon Trigger Performance Prototypes

25ns bunch identification timing from anode wires



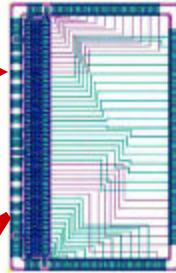
Bend coordinate position to 1mm from cathode strips



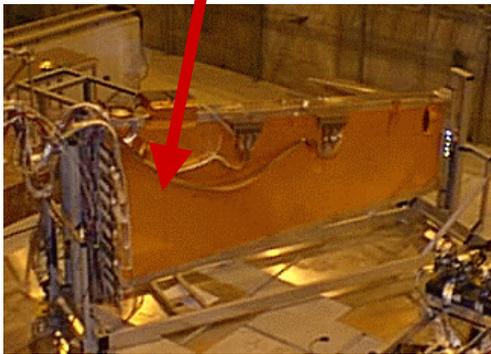


1998 Trigger Performance Prototype Modules

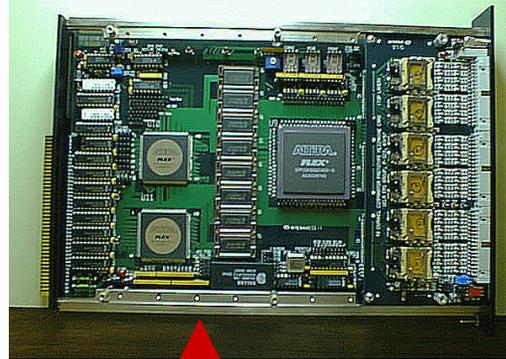
Comparator ASIC



Comparator Board

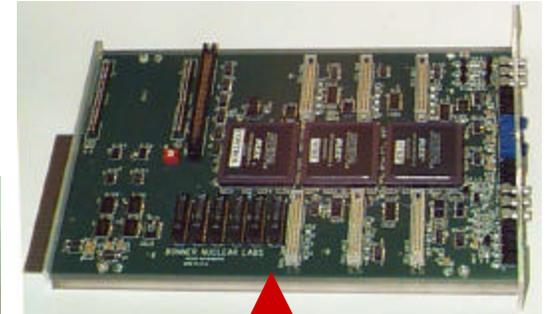


CSC Chamber

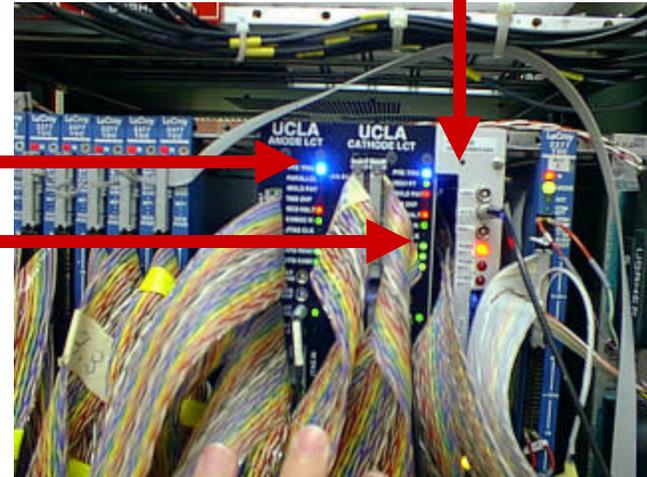


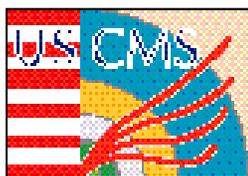
Anode LCT

Cathode LCT



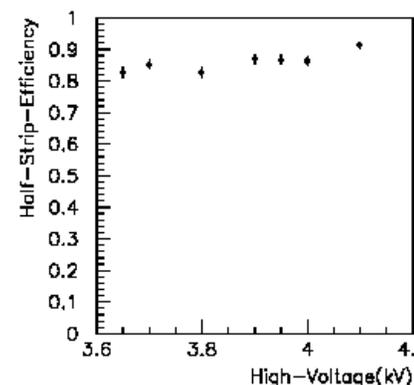
Trigger Motherboard



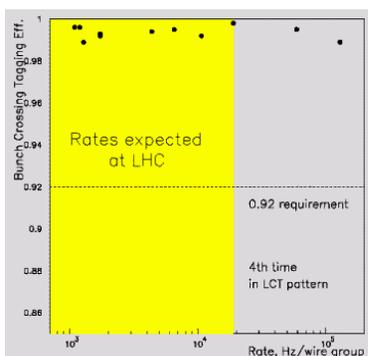


Trigger Results from 1998 CERN Test Beam

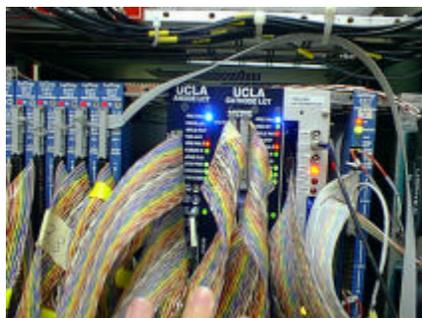
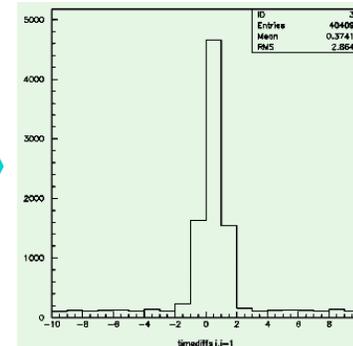
Cathode LCT for position:
half-strip eff. ~90% per layer
~0.1 strip/chamber position resolution



Anode LCT for timing:
bunch crossing efficiency 99%
works at 7x max LHC rate



Cathode-anode timing at TMB:
+/-1 bunch xing 98% efficient



Electronics was reliable, no pickup noise, etc.

Prototypes meet the CMS design criteria in all aspects

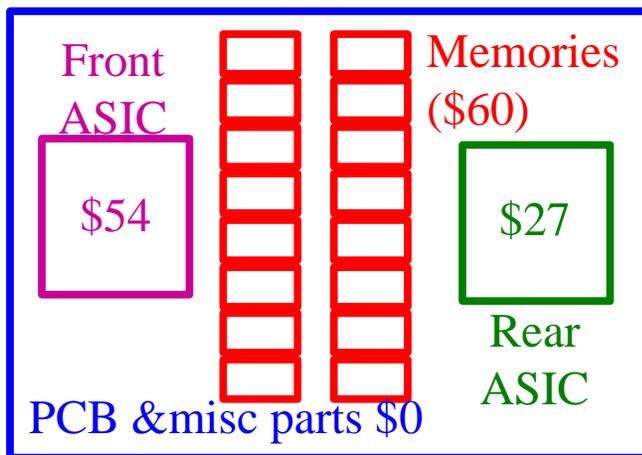


1997 LCT Cost Estimate

- The original plan was for on-chamber, 96-ch LCT cards
- The gate array market changes rapidly, so the original cost estimate for trigger electronics required technology extrapolation

1997 Cost Estimate:

- 96-channel circuit integrated into FE boards



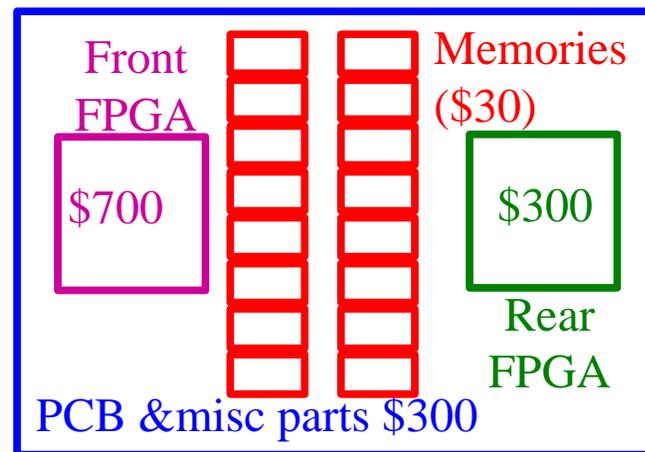
\$1.46/ch = \$141/96 channels

**3204 cards (1728 strip, 1476 wire)
+spares for 3 stations**

Total cost = \$0.5M

1998 Performance Prototype:

- 48-channel circuit
- 8"x11" board size



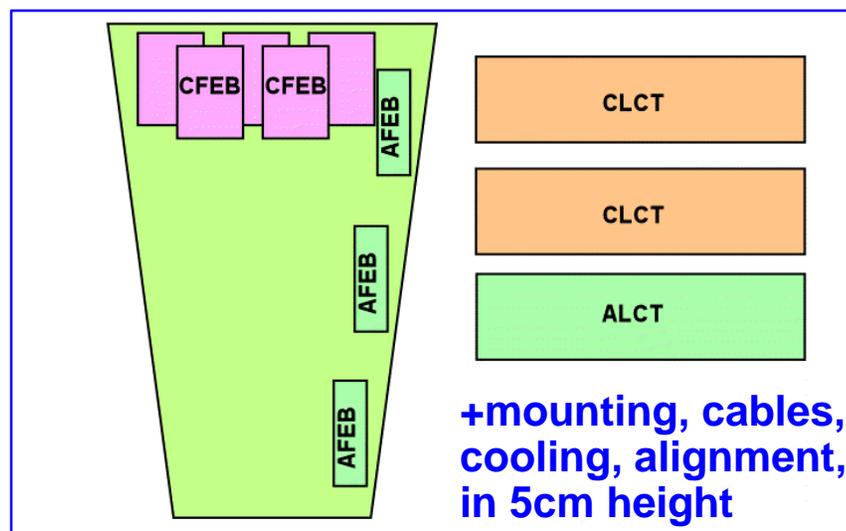
\$28/ch = \$1330/48 channels

Total cost = \$9M



Moving from the Performance to Engineering Prototype:

- **Add elements to complete CMS-ready design**
 - readout of input data bits
 - multi-buffering
- **Decrease per-channel board size**
 - 1998 prototype: 48 channels in 8"x10"
 - 480 channels requires 800 in², too much for smaller chambers
 - For example, ME1/2:





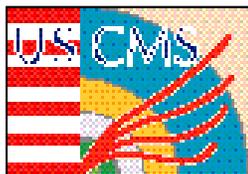
Transition to Engineering Prototype Electronics

Primary cost driver:

- High I/O pin count for gate arrays (FPGA)
- Unavoidable in FPGA-RAM lookup-FPGA technique

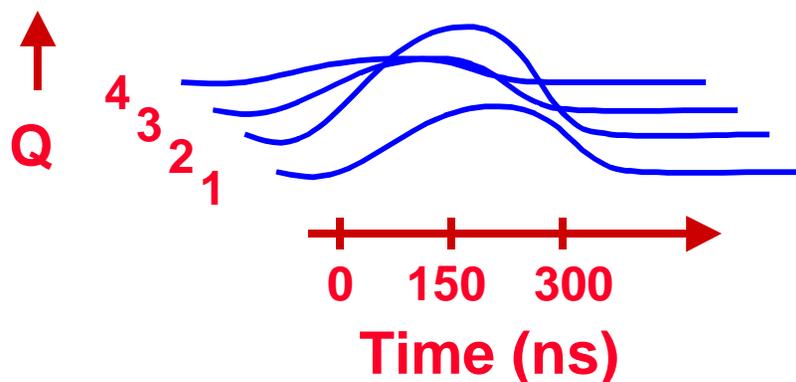
Steps taken:

- 1 - **DONE:** Invent data compression for cathode ASIC to reduce cathode inputs by 4:1
- 2 - **DONE:** Produce a new all-in-one design by replacing RAMs with FPGA internal look-up tables
- (3 - **NEXT STEP:** use small, simple, and less expensive FPGA chips working in parallel for anode LCT card.)

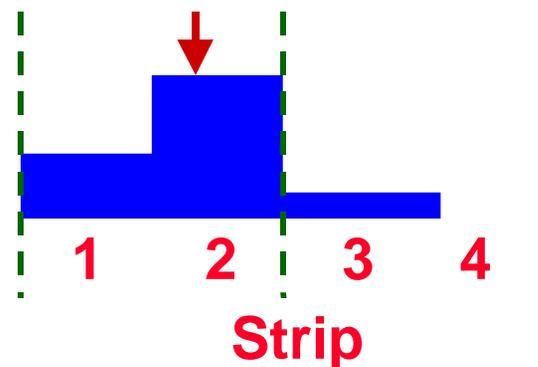


Step 1 - Lossless Data Compression for Cathode Trigger ASIC

1) Strip charge vs. time:



2) Charge at peak time:



3) Half-strip parallel bits:

T (ns)	0	1	2	3	4	5	6	7	8
125	0	0	0	0	0	0	0	0	0
150	0	0	1	0	0	0	0	0	0
175	0	0	0	0	0	0	0	0	0
200	0	0	0	0	0	0	0	0	0
...									

4) Serial output:

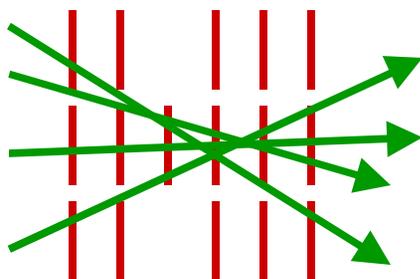
T (ns)	0	1	2	3
125	0	0		
150	1	0		- "Distrip" hit
175	1	0		- Strip 2 hit
200	0	0		- Left side
...				



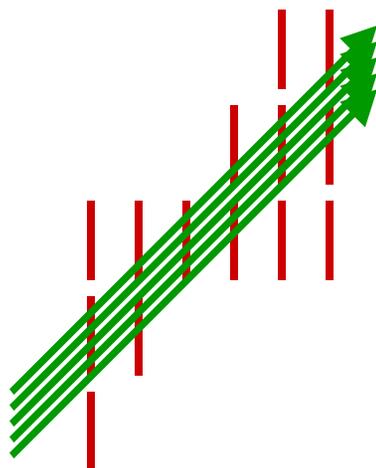
Step 2 - New All-in-one Design (Prototype built August 1999)

480-channel module on 12"x17" board

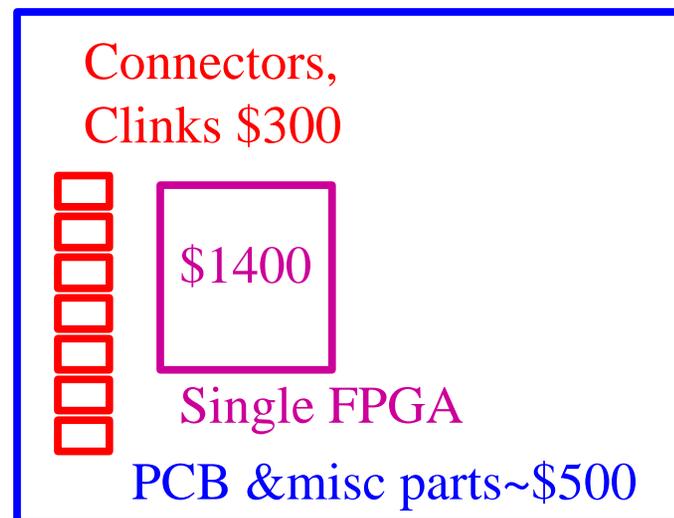
**Cathode
patterns**



**Anode
patterns**



Board Layout



360 cards plus spares, \$2200/480 channels = \$4.58/ch
Resulting cost ~\$1M for cathode



Cost Changes in Endcap Muon Electronics

Other electronics changes:

- An additional round of prototyping
- High-tech cables needed for small “skew” time
- Crates on muon iron periphery

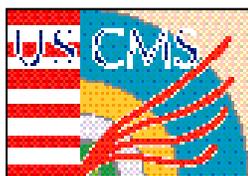
Initial un-optimized analysis:

		NEW (M\$)	OLD (M\$)	NEW-OLD(M\$)
1	Prototype DMB,TMB,CLCTB,ALCTB	0.89	0.42	0.47
2	CLCTB, ALCTB production	2.06	0.95	1.11
3	Cables (FEB-Crate)	0.89	0.28	0.61
4	VME Crates	0.34		0.34
5	DMB/DDU production	0.82	0.54	0.28
6	TMB/CCB production	0.92	0.88	0.04
7	CFEB production	1.58	1.35	0.23
8	AFEB production	1.27	1.07	0.20
9	Optical Links	0.24	0.22	0.02
10	Installation	0.19		0.19
	TOTAL	9.20	5.71	3.49



Cost Optimization

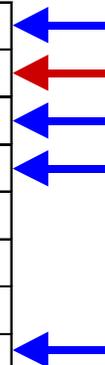
- **Largest potential optimization in anode cards**
 - **Drastically simplify front-end boards**
 - Just 16-ch preamp/discriminators with minimal support
 - **Keep anode LCT on-chamber**
 - Reduce size with all-in-one LCT chips
 - Keep cost down with simple small LCT chips working in parallel
 - Eliminate expensive high-tech cables to anode LCT cards
- **Other potential cost savings**
 - Put Trigger Motherboards (\$0.5M) on CLCT cards
 - Reduce number of peripheral 9U crates from 96 to 48



Revised Cost Changes in Endcap Muon Electronics

- Simplified front-end anode cards
- On-chamber Anode LCT cards
- Combined CLCT and TMB cards
- Reduced crates and cables
- Relevant items:

	NEW (M\$)	Baseline (M\$)	NEW-Baseline(M\$)
Prototype DMB,TMB,CLCTB,ALCTB	\$0.85	\$0.50	\$0.35
CLCTB, ALCTB production	\$1.90	\$0.95	\$0.94
Cables	\$1.22	\$0.68	\$0.53
VME Crates	\$0.17		\$0.17
DMB/DDU production	\$0.82	\$0.55	\$0.27
TMB/CCB production	\$0.56	\$0.89	-\$0.33
CFEB production	\$2.87	\$2.60	\$0.27
AFEB production	\$0.66	\$1.37	-\$0.71
Optical Links	\$0.24	\$0.22	\$0.03
Installation	\$0.19		\$0.19
TOTAL	\$9.48	\$7.77	\$1.71





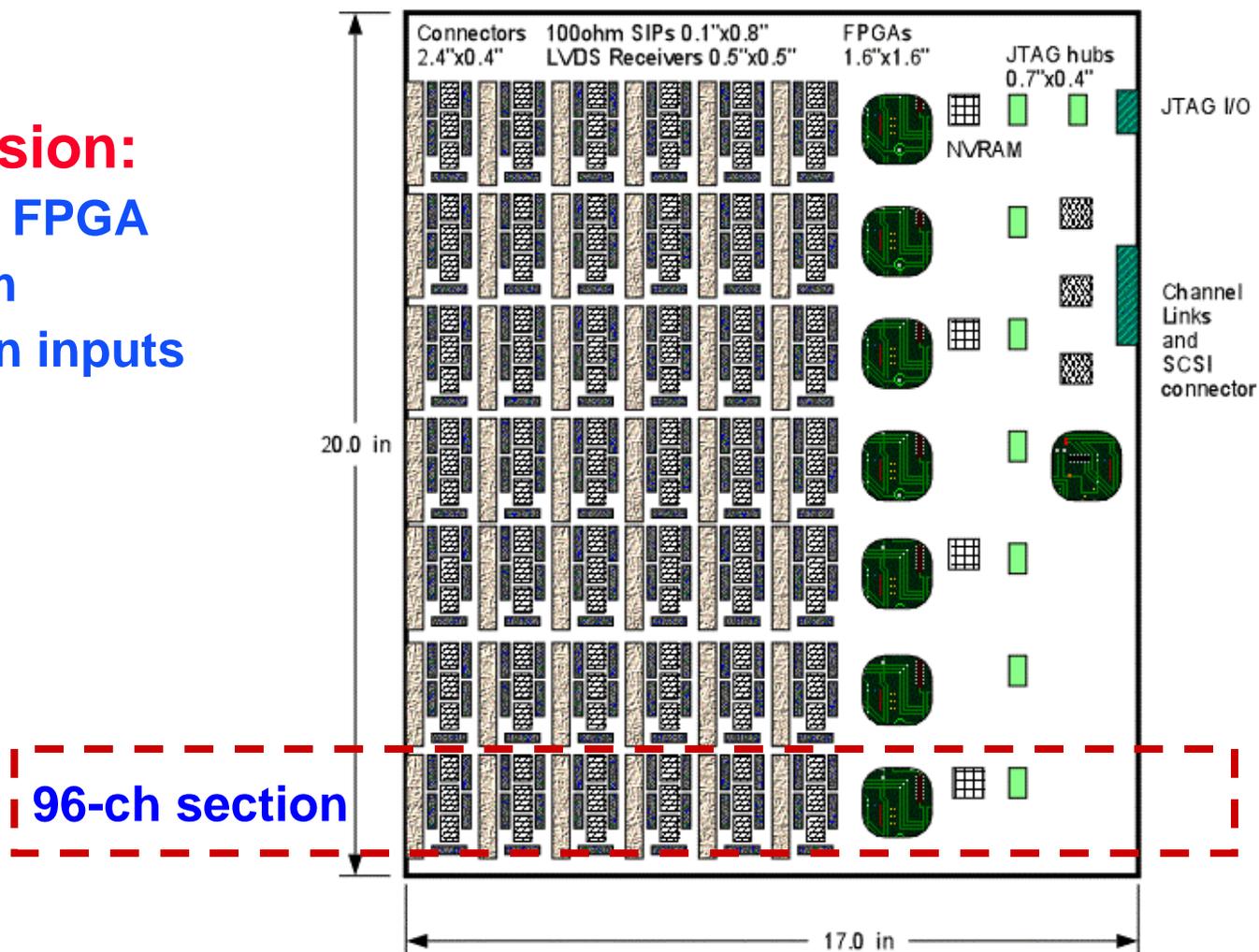
Step 3 - Revised On-chamber Anode LCT Card Layout

- 288, 384, 672 ch versions

- Shown is

672 ch version:

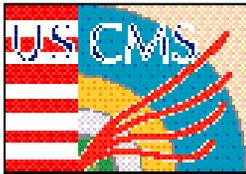
- 96ch per FPGA
- 43x51 cm
- 42x40-pin inputs
- 13 Watts



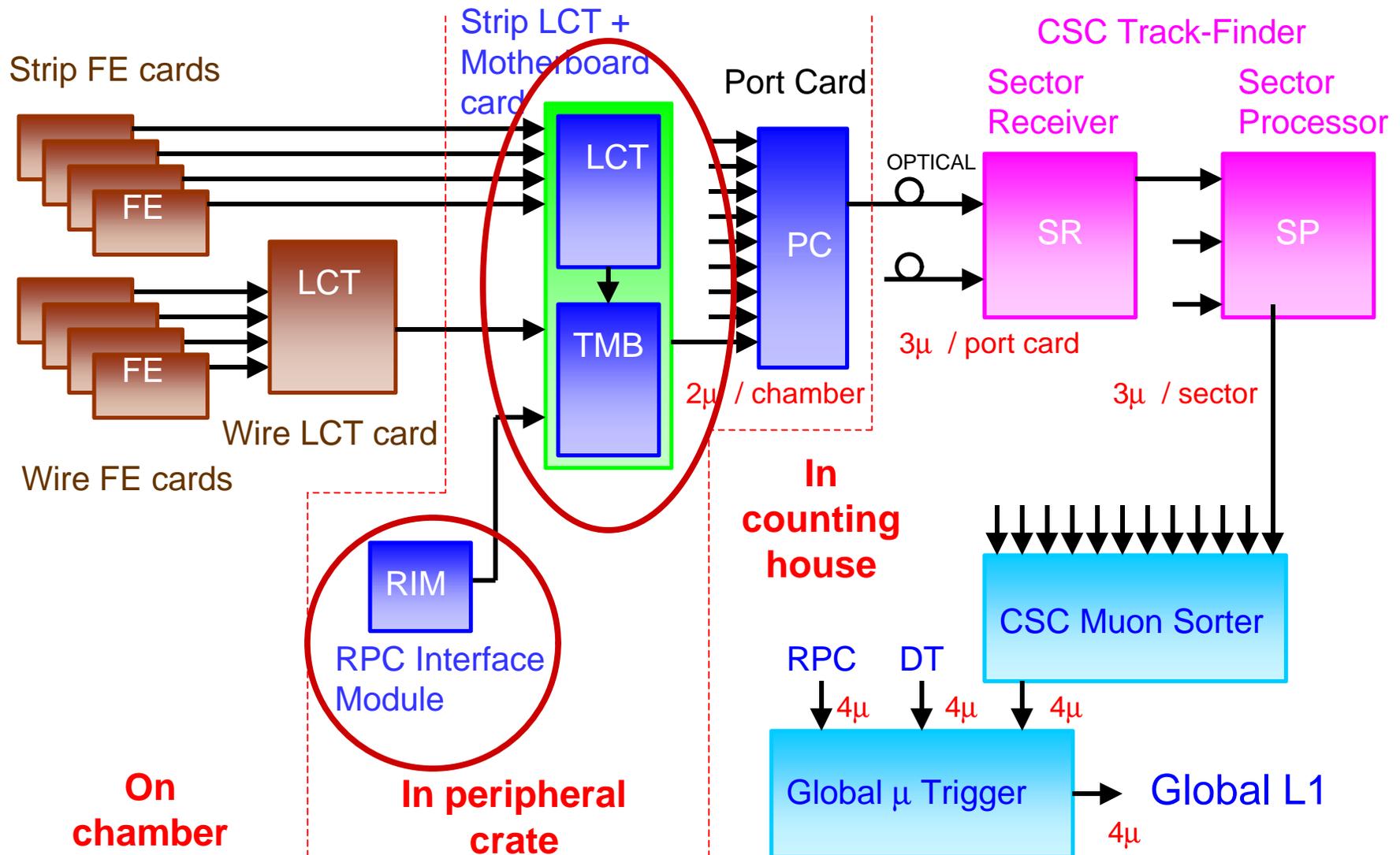


Revised On-chamber Anode LCT Card

- **Technically feasible**
 - 96-ch logic has been simulated and fits “inexpensive” gate arrays.
 - Straightforward to divide logic between FPGAs
- **Little change in on-chamber space use**
 - Space is dominated by connectors and level converters
- **Demonstration**
 - Prototype to be built by Feb. 2000



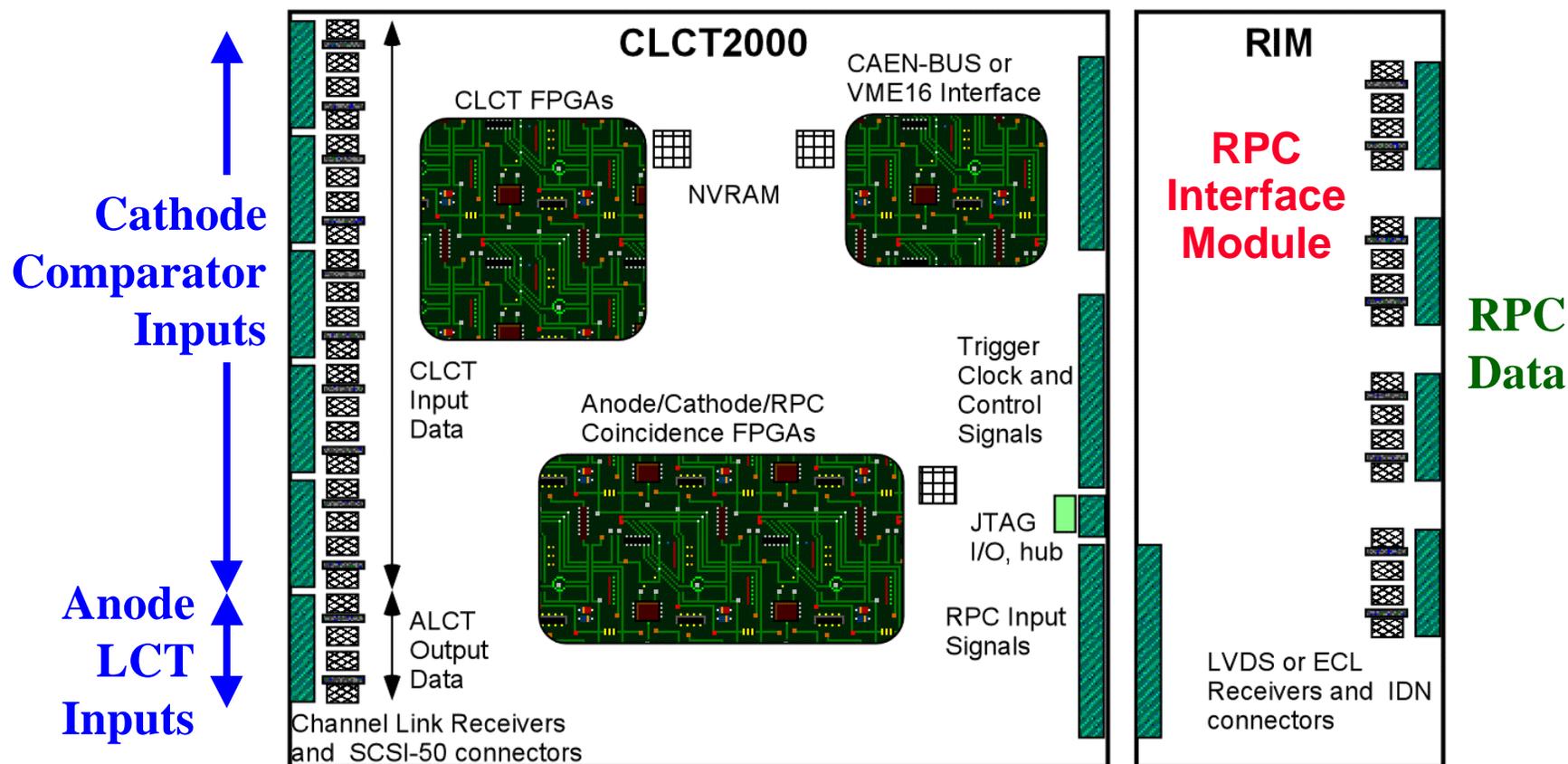
Combining CLCT and TMB

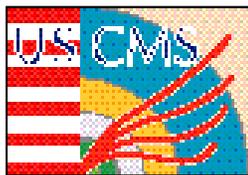




Combining CLCT and TMB

- VME 9U module with anode coincidence and capability to add RPC coincidence





Summary

- **It is necessary to move electronics into peripheral crates**
 - Solves on-chamber space problem
 - Other major benefits for power and cooling, access for maintenance and DAQ connection, and timescale for installation
- **The Feb. 1999 Project review supported this, even though it was known that cost would increase**
- **A preliminary cost estimate (\$1.71M) has been made**
- **Existing major milestones for on-chamber electronics are unchanged**
- **New milestones for off-chamber electronics are consistent with installation in 2004**
- **The design and costing will be finalized by October and then a change request will be presented to the PMG**